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Design, Implementation and Development of a digital AM Receiver Using TDA 1072 IC

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Abstract:

The process of finding cheaper and better means of implementing electronic solutions is the goal of modern technology. This paper focuses on finding an alternative means preferably digital and firmware based on design and develop a digital AM receiver using TDA1072. The Amplitude Modulated receiver circuit consists of an antenna, AM demodulation unit with signal indicator output, digital tuning circuit (frequency Synthesiser), integrator, differential amplifier, frequency divider and microcontroller output. The AM demodulator IC uses balanced full-wave detector method for demodulation. Internally, it has a full wave rectifier circuit that gives signal strength indication output, and frequency oscillation that can give audio output as well. The ADC converter of a microcontroller (PIC 16F877) converts the output signal into digital. This system will display the frequency received by dividing the frequency from the oscillator, and this will be fed into PIC16F877 to give station frequencies that will be locked into. An audio output through speaker is incorporated and the station programmes is heard. Tuning to different stations is done using PLL circuit which generates a local oscillation via a varactor for balanced full-wave demodulation.

Keywords **—Amplitude Modulation, Microcontroller, Frequency Synthesizer, Full wave Detector**

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I. INTRODUCTION

The use of microcontroller for electronic communication became very popular among researchers these days. In conventional AM radio receivers, selection of stations and channels tuning are done manually, which involves using electromechanical system that generates the appropriate frequency of a local oscillator by means of an inductance-capacitance oscillator (2) The problems involved in manual tuning are (i) accurate tuning depends on the user's hearing capability.(ii) the output of a continuously tuneable local oscillator (LO) is subject to frequency drift which means occasional retuning may be necessary (5). Stable, rapid and accurate frequency selection is available today using frequency synthesizers with microcontroller. Digital tuning with microcontroller involves using a frequency synthesizer which have four basic components. (i) phase lock loop (ii)voltage controlled oscillator (iii) programmable divider (iv) loop filter

The AM Broadcast service in Nigeria and many other countries is implemented on 10 kHz channel steps with center frequencies 540 kHz through to 1700 kHz, and carrier power levels from 250 watts to 50 kilowatts (2). The AM receiver used in this work is a AM superheterodyne receiver that can pick up any AM radio station. An AM superheterodyne receiver detects amplitude variations in the radio waves at a particular frequency, converts a received amplitude-modulated wave back to the original source information, which is the process of demodulation, It then amplifies changes in the signal voltage to drive a loudspeaker or earphones (1), in other words AM receiver is capable of receiving, amplifying and demodulating an AM radio wave (1).The aim of this work is to design and develop a simple, affordable and digital AM receiver using TDA 1072 IC. The system uses a digital procedure, a microcontroller for the control system. TDA1072 forms the heart of the measuring equipment having internal voltage controlled oscillator and a received signal strength output

II. METHODS

The complete block diagram of a digital AM receiver is shown in figure 1. It was broken down into stages and they are: An Antenna, AM radio receiver circuit, Controller circuit with user input and output interface, Frequency synthesizer (Programmable divider circuit, Phase lock loop and reference oscillator circuit), Audio amplifier circuit. The digital AM receiver is designed around a TDA1072 radio chip and a PIC16F877 microcontroller as the controller chip. A frequency synthesizer is used to enable digital tuning between radio stations. An LCD (liquid crystal display) displays radio stations in kilo-hertz and also displays field strength in decibel micro-volts. The keypad is the user interface for communicating a change in radio station to the receiver. An audio amplifier is added, and completes the circuit such that the user can listen to the radio station under observation. From figure 1, the system works as follows. An antenna A1 intercepts an AM radio wave and supplies the signal to a radio frequency amplifier of an AM receiver chip. The AM radio receiver receives rf signal, amplifies it and demodulates it to an audio frequency (AF) signal which corresponds to a modulated broadcast signal. The detected audio frequency output is passed through an AF pre- amplifier of AM receiver to audio amplifier and to a speaker. The controlled oscillator signals is generated from frequency synthesiser and fed into the mixer of AM receiver chip for mixing with the RF signal. The Local oscillator signal from AM receiver chip is supplied to a programmable divider, the divider divides the frequency fx of the channel signal with a predetermined ratio N, thereby converting the channel signal into a first frequency. Divided signal having a frequency of fx/N is fed into a phase detector of PLL. The signal from a field strength indicator is amplified and fed through the microcontroller to the display. The control key input the frequency of the channel station, and it will display in the LCD. The audio signal is taken and re-amplifies before it is fed to the speaker.

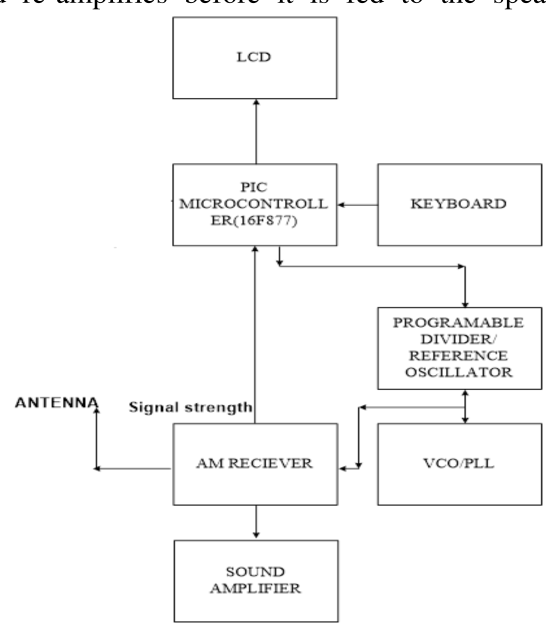

Figure 1. Block diagram of a digital AM Receiver

A. *Description of AM receiver Radio circuit*

TDA 1072 performs all the main function of an AM superhet radio receiver including RF Amplifier, Local Oscillator, Mixer, Detector, AF Amplifier, AGC system and Field strength indicator as shown in figure 2. The TDA 1072 integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver (data Sheet). The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV

*i) Antenna, Gain-controlled RF and mixercircuit:*From figure 3, A monopole antenna of 50 ohms receives the AM signal. The signal is sent to pin 14 of RF amplifier via capacitor C19. A double balanced mixer provides the IF output at pin 1of U0

*ii) Local Oscillator:*Frequency synthesizer generates oscillation frequency (4) and it uses varactor D1, and a parallel tank (consist of coil L1, and capacitor C15 and C17) connected between pins 11 and 12 of U0. Controlled oscillator output from pin 10 of U0 is fed to programmable divider through transistors Q1 and Q2 and a comparator(LM393) U32 which are used to amplify and convert the analogue signals (sine wave) to digital (Square wave) to form input signal to programmable divider. To design a n Inductor L1, a local oscillator of AM operates at 455kHz above the wanted incoming signal frequency. The local oscillator needs to be tuned to a range 990 i.e (535 + 455) kHz to 2100 i.e (1645 + 455) kHz. The tank inductor L1, can be designed using Waller's formula in equation 1.

$$L = \frac{N^2 d^2}{18r + 40l} \qquad 1$$

From the circuit we have; Number of turns $(N) = 4$ turns, Diameter$(d) = 8$mm, length $(l) = 7mm$, capacitors $C1 = 1nF$ and $C2 = 100nF$. For 1-inches gives 25.4mm therefore,

Conversion from mm to Inches

$$d = \frac{8mm}{25.4mm} = 0.315\ inches \qquad 2$$

$$l = \frac{7mm}{25.4mm} = 0.2756\ inches \qquad 3$$

$$L_1 = \frac{4^2 \times 0.315^2}{18(0.315) + 40(0.2756)} = 0.095 \qquad 4$$

L1 = 95μH ,.

iii*) IF filter and IF amplifier:* The intermediate frequency signal from the mixer output via pin1 of TDA1072 is filtered through IF filter show in figure 2. In Designing of IF filter equation 5 was used in designing IF filter,

$$f_c = {}^{1}\!/_{2\pi\sqrt{LC}} \qquad 5$$

Where f_c is the centre frequency, L is the inductor and C is the capacitor.455kHz was selected as centre frequency, figure 2 shows the IF filter, consist of two pole ladder crystal filter X1 and X2 of 455kHz, a matching transformer TR1, capacitors C23 and C24. The matching transformer has 13 turns on the primary coil and 9 on the secondary coil. A trimmer capacitor C23 is used to resonate the inductance of 31μH of the primary coil of TR1. C29 was calculated to be 3.9nF

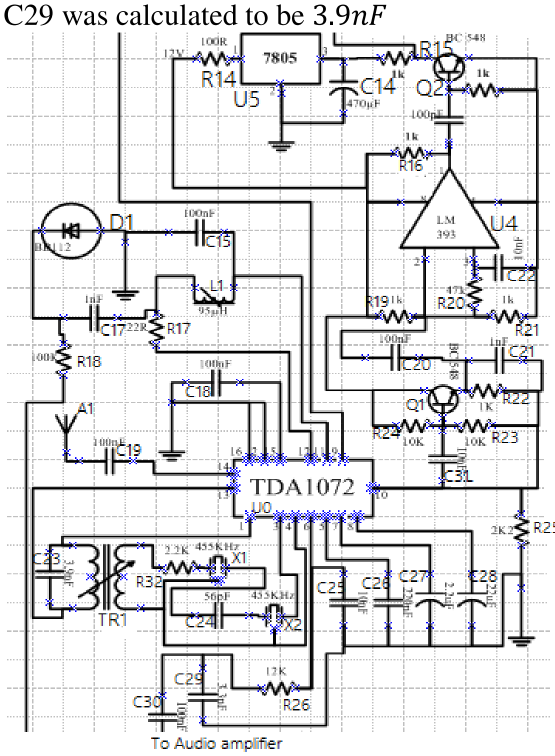

Figure 2. AM Radio Receiver Circuit

iv) Detector and AF pre-amplifier: Figure 2 the full- wave balanced envelop detector is used for demodulation of the intermediate frequency to audio frequency signal. The audio frequency signal is amplified by AF pre-amplifier. The audio filter is made up of capacitor C29, C30 and resistor R26. The AF output voltage at input signal $50\,\mu V$ is 130mV, (Data sheet of TDA 1072)

v) AGC amplifier: The Automatic gain control (AGC) amplifier gives out a control voltage that is proportional to the carrier amplitude. The AGC voltage is fed to the RF and IF stages via suitable AGC delays.

vi)Field strength indicator output: A buffered voltage source from the IC TDA 1072 provides a high-level field strength output signal.

B. *Frequency Synthesizer*

A frequency synthesizer is a device (an electronic system) that generates a large number of precise frequencies from a single reference frequency. This paper is based on amplitude modulation whose frequency spans from 535 kHz to 1605 kHz. Figure 3 shows a modified frequency synthesizer block employed in this work. Apart from the standard divide by N value, a fixed divide by M value of 2 is used. N is between 535 and 1605 reference frequency is 500 Hz. Frequency output will be M x N x reference frequency. The TDA1072, U0 is an AM receiver used, the front end of the receiver uses a mixer and an intermediate frequency such that to choose a given station, let say 1000kHz. The output of the mixer with the input signals X and Y is the subtraction of the two signals and the addition of the two signals. The TDA1072 always expects a result from the subtraction as 455 kHz, hence to tune to a station of 1000 kHz representing signal X, and Y signal will be 1455 kHz from the local oscillator is needed. From the above analysis the N value needs to be compensated for the intermediate frequency which is 455 kHz, the new N value is; (535 + 455) to (1605 + 455) i.e. 990 to 2100.

The programmability from 990 to 2060 is achieved by a 12 bit counter $2^{12} = 4096$ using three 4-bit LS74161 (U33, U32 and U31). The LS74161 is a 4 bit synchronous, pre-settable counter. (see figure. 4) Moreover, in order to achieve counting programmed inputs for 990 to 2100. Firstly, all inputs are cleared to zero, then decimal number of 990 using inputs of D0 – D3 of three cascaded counter is loaded with preset value at 990 and counting starts from 990 to 2100, then inhibit.

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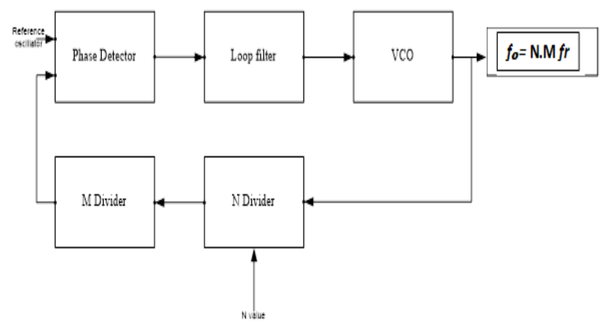

Figure 3. Modified frequency synthesizer block employed in this work

i). *Timing of three cascaded LS74161- 12 bit counter.*

The two ICs required for the timing of a 12 bit cascaded counter LS74161 are SN7408 and NS7414. (See in figure 5). The SN7408 is a quad 2 input NAND gate,(U8a and U8b), while the LS7414 is a hex Schmitt trigger inverter, U10 both form the timing for the enable pin ENP (pin 7) and load pin (pin 9) of LS74161-a 12 bit counter. NAND gate (U8a), of the SN7408 is used to convert the cascaded counter from 12 bit to divide by N counter where the maximum count before re-load is 4096. The NAND gate (U8a) output clocks the DM7493A counter used as divide by 2 (representing the M divider). The second NAND gate U8b of NS7408, and the SN7414 (5 gates U10) are used to create a timing such that a reloading of the 74161 can be achieved as described in reload diagram. A reload signal occurs at the 4090 counts and this is asserted high on pin 6 of the SN7408

(U8a), this serve as reload signal. U8b of SN7408 and U13of SN7414 forms a two input NAND gate. (see in fig 4 and 5)

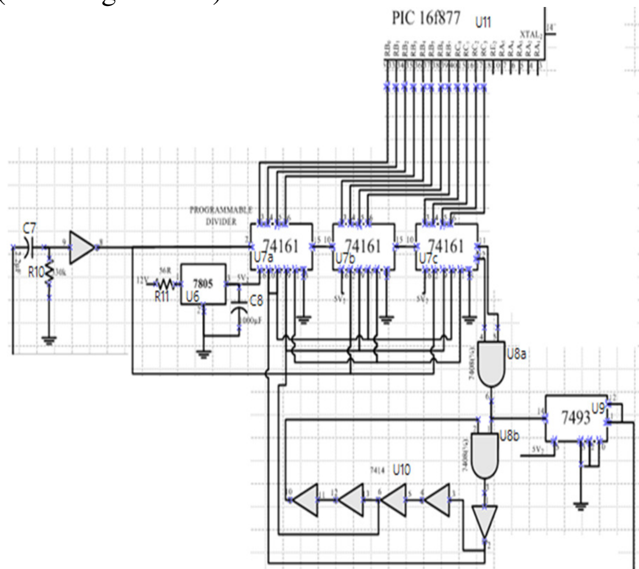

Fig. 4. Programmable Divider Circuit

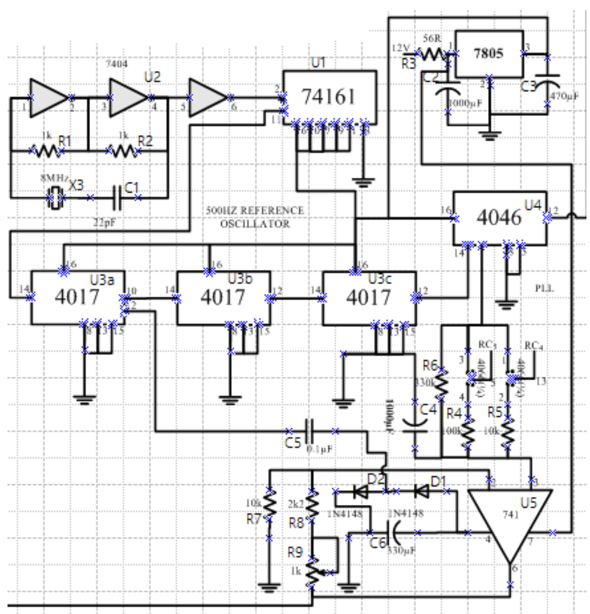

Fig. 5. Reference Oscillator and PLL Circuit

i) Reference Oscillators

The reference oscillator is 500 Hz, to achieve this, a crystal oscillator of 8 MHz, X3 was obtained and divided down to 500 Hz. The circuit is shown in figure 5. The NOT gate 7404, (U2) serves as amplifier (buffer) for the crystal to oscillate and the two1kΩ resistors (R1 and R2) are the feedback resistors for the amplifier. LS74161,

U1 is a 4 bit counter and it divides 8 MHz, X3 by 16 to get 500 kHz, Also three 4017 decade counters (U3a, U3b and U3c) are cascaded to form a divide by 1000 counter, the result is that 500 KHz is divided by 1000 to get 500 Hz, on pins 12 of the 3rd 4017, U3c.Pin 12 of 4017 counter U3c carries over the divide by 10 output to clock pin 14 of counter U4 and pin 12 of counter U clocks pin 14 of the third counter U21, then the output is fed on pin 14 phase comparator II of the PLL 4046 input as reference oscillator of 500Hz.The output of VCO (from TDA1072 AM receiver) is fed back to the phase comparator II second input ,through a programmable divider programmed to divide by any number from 990 to 2100. The loop locks when the frequency fed back is equal to 500Hz of reference oscillator frequency. A simple RC filter is employed as the loop filter. Where C12 is fixed at 1000µf, the value of R varies via a digital switch between 10 kΩ, 100 kΩ and 330 kΩ. The CD4066 analogue switch is controlled by the PIC controller. The need for using different loop is to ensure fast lock and smooth lock. The centre frequency of the low pass filter is given as

$$f_c = {}^{1}/_{2\pi RC} \qquad 8$$

$R_{12} = 10k\Omega,$

$$f_c = {}^{1}/_{2 \times \pi \times 10 \times 1{,}000{,}000{,}000} = 0.015Hz \qquad 9$$

$R_{15} = 100k\Omega,$

$$f_c = {}^{1}/_{2 \times \pi \times 100 \times 1{,}000{,}000{,}000} = 0.0015Hz \quad 10$$

$R_{16} = 330k,$

$$f_c = {}^{1}/_{2 \times \pi \times 330 \times 1{,}000{,}000{,}0000} = 0.0048Hz \quad 11$$

The output of the phase comparator/detector is amplified using LM 741 OP-AMP, A noninverting amplifier configuration is used. The gain of the stage is;

$$G = 1 + {}^{R_F}/_{R_{44}} \qquad 12$$

Where R_F is 2.2 kilo-ohms (R_{17}) and 1 kilo-ohms(R_{V2}) variable in seriesR_{18} is 10 kilo ohms,

$$G = 1 + {}^{(2.2\,+\,1)}/_{10} = 1 + {}^{3.2}/_{10} = 1.32 \qquad 13$$

This gives a gain of less than 2.

C. Controller circuit with user input and output interface

Figure 6 shows the PIC circuit with the interface connection. The pic16f877 U9 is a central processing unit, a complete computer on a chip. It has three types of memory which are flash program memory, electrically erasable memory and static random access memory. Flash program memory is used for storage of program codes through the use of a PIC programmer., while electrically erasable memory is used to store results from program execution that needs to be retained even after power outages and static random access memory is used during program execution; data here is lost once there is a power outage.

The pic16f877 has 33 inputs and output pins that can be individually configured as inputs or outputs and they are group as: PORT A (6 input/output), PORT B (8 input/output), PORT C (8 input/output), PORT D (8 input/output), PORT E (3 input/output). These ports have been assigned to the various tasks in the circuit. PORT A bit 0 is configured via firmware as an analogue input for analogue to digital conversion. The PIC is equipped with an eight channel, one channel is used to convert received signal strength which the tda1072 generates in analogue form to digital, which can then be displayed on the LCD unit. Data is written for display to the LCD using ASCII (American Standard Code for Information Interchange) codes. Pins 15 and 16 are the supply lines for backlight for the screen display. Values for voltage and current for backlight as specified in the manufacturer's datasheet are:

$Voltage\ = 4.2V, Current\ = 15mA\ (typical\ value).$

A series resistor is therefore needed to connect to a 5V supply. The value of the resistor is given as:

$$R\ = \frac{(voltage\ supply - voltage\ backlight)}{current\ backlight} \qquad 14$$

$$R\ = \frac{(5\ -\ 4.2)}{0.015}\ = 53.3\ ohms \qquad 15$$

A value of 180 ohms was chosen to obtain overall minimum current consumption. Using 180 ohms the current consumed by the backlight:

$$current\ I\ = \frac{Voltage\ supply - voltage\ backlight}{resistor} \qquad 16$$

$$= \frac{(5-4.2)V}{180\Omega} = 4.4mA \qquad 17$$

PORTA bits 1, 2, 3, 4, 5 and PORTE bit 2 are used for the user keypad.

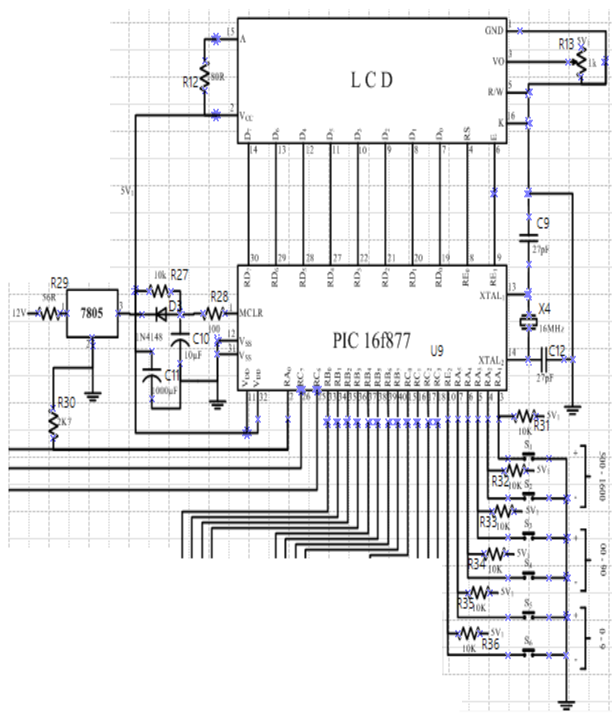

Fig. 6. Controller Circuit

D. Audio Amplifier

The audio amplifier is shown in figure 7, uses ic LM386 power amplifier designed for use in low voltage consumer applications.(Data Sheet) The gain is internally set at 20, but the additional gain value from 20 to 200 was added using an external resistor and capacitor between pins 5 and 3

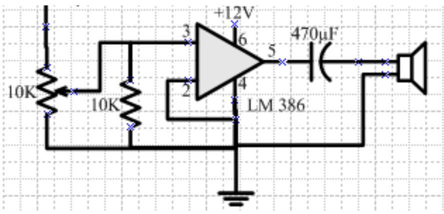

Figure 7. Audio Amplifier

E. Power supply

The power supply circuit shown in figure 8 powered the whole system from an 18 volts rechargeable battery source. A transformer is provided to charge the battery. The voltage is then regulated to 12 volts and 5 volts for each stage using voltage regulator 7805.

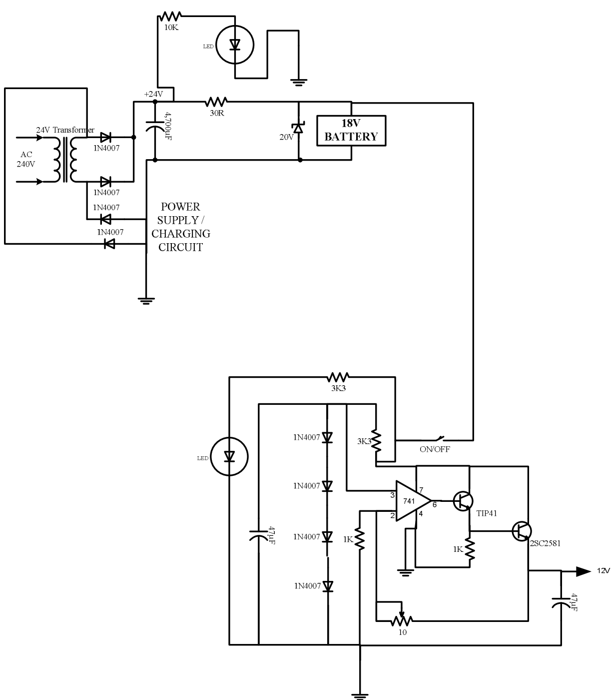

Fig. 8Power supply circuit

III IMPLEMENTATION AND TEST

A signal generator with modulating input and an oscilloscope were used to verify circuit integrity. The VCO output at pin 10 of the TDA1072 was connected to the oscilloscope set to a time-base of 0.2µs and Voltage sensitivity of 20mV per division. The expected output waveform should have a peak to peak of about 100 mV according to the manufacturer's datasheet. The input of the VCO was then tuned manually using a potentiometer and the output of the oscillator was observed to vary from 800 kHz to 2100 kHz which covers the expected range of 990 kHz to 2060 kHz needed to span the AM spectrum. Figure 9 shows the output of VCO signal. The VCO output was amplified and converted to square waveform digital signal this was also verified on the oscilloscope.

The next test was mixer output test, the signal generator was set to 1MHz and a 1 kHz signal was used to modulate. This signal attenuated sufficiently was connected to the RF input of the TDA1072 at pin 14. The VCO was also tuned manually to 1455 kHz. The output of the TOKO coil was then observed on the oscilloscope set to a time-base of 5µs and voltage sensitivity of 5mV per division, the coil until when a clear 455 kHz difference signal was observed on the oscilloscope. Figure 10 shows the mixer output at 455 KHz

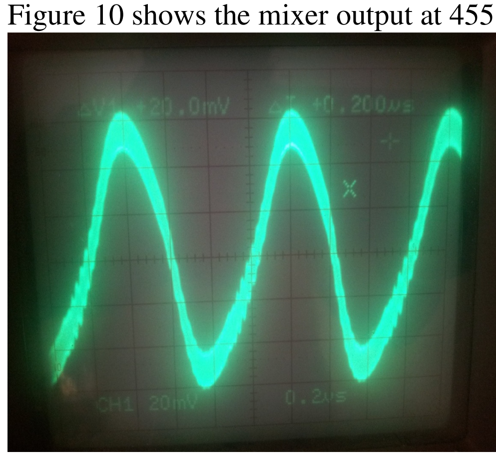

Fig. 9 VCO output

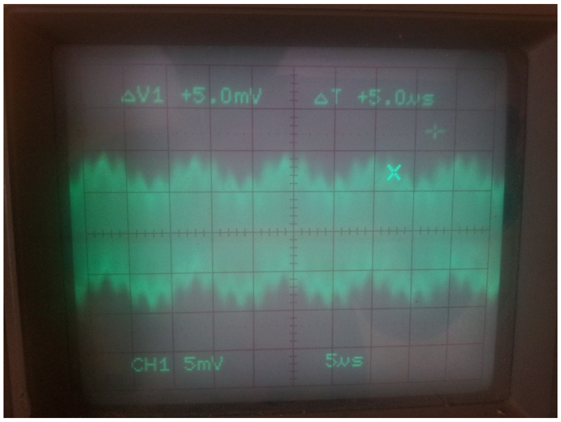

Figure 10.: ***mixer output at 455 KHz***

The reference oscillator is 500 Hz. In a test for reference oscillator of 500Hz,. The bench power supply, was fixed at 5V and the oscilloscope was used to test the 8 MHz oscillator and output of the decade counters which give final output of 500 Hz. The oscilloscope was set to a time base of 0.5µs and voltage sensitivity of 5V per division for the 8 MHz test, for the 500 Hz a time base of 0.5ms is used while maintaining previous volts per division. Figure 11 shows the 500Hz reference oscillator output

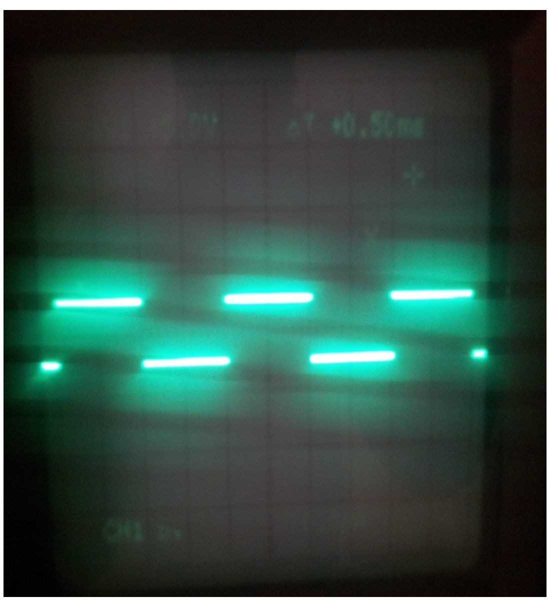

Figure 11. A 500Hz reference oscillator output

IV. PERFORMANCE TEST OF AM RADIO RECEIVER

On completion of the design and construction work, certain performance test was carried out by tuning the constructed AM radio receiver to frequency of 756kHz, the Broadcasting Corporation of Oyo State, Ile Akede, Bashorun, Ibadan, transmitting at the frequency of 756kHz. The radio receiver is capable of detecting the field strength of the signals from that station. The Broadcasting Corporation of Oyo State (BCOS) in Ile Akede, Bashorun, Ibadan, transmitting at the frequency of 756kHz. The locations for the test are; Bodija market, University of Ibadan, Ibadan airport and International institute of Tropical Agriculture. Table 1shows the data collected from four different locations in Ibadan, the distances from the AM transmitter at Ile Akede, Ibadan, Oyo State and the corresponding AM field Strength.

Table I: Table of the data collected from four different locations in Ibadan, with their distances from the AM transmitter at Ile Akede, Ibadan

Location	Distance from AM transmitter (km)	Field strength measurement from test AM meter (dBµV)
Bodija Market	2.9	50.23
UI	5.8	48.72
Nigerian Brewery	7.0	44.25
Ibadan Airport	8.0	45.73
IITA	10	42.50

V. RESULT AND DISCUSSION.

The constructed AM radio receiver performance was evaluated in terms of sensitivity and selectivity. Table 1 shows the data of the distances and the corresponding AM receiver field Strength from the AM transmitter at Ile Akede, Ibadan, Oyo State.

Figure 12 also shows the result of field strength against distance in km, as the receiver moving away from the transmitter sothe distance increasesand there is gradual decreased in the field strength,

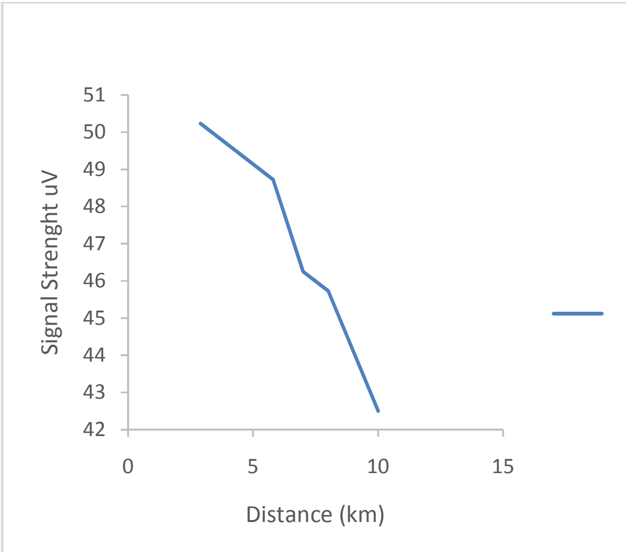

Figure 12: Graph of field strength (dBµV) vs distance (Km)

V. CONCLUSIONS

An AM radio receiver is capable of receiving AM signals from any AM broadcasting transmitters with centre frequency of 500kHz to 1650kHz, bandwidth of 10khz and gain control from 0 – 120dBµV was designed, constructed and tested. The system consist of an antenna, AM demodulation unit with signal indicator output, pre-amplifier, frequency divider, tuning circuit comprising of a phase lock loop (PLL), integrator, differential amplifier, microcontroller output with serial communication interface and a varactor. The AM receiver using digital tuning (frequency synthesisers). Frequency synthesiser helps to overcome some problem of accuracy and stability of signals.

A performance test was conducted with this radio receiver. The work testing exercise was conducted in five different locations in Ibadan city, Oyo State. The result shows that the meter works perfectly, it's audible and clear, the signals fade away with distance.

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