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Design and Analysis of Low Power GDI Based Johnson Counter

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Abstract:

A low power design of Johnson counter is proposed which provides huge depreciation in the power dissipation. Clock gating technique is used to suppress the unwanted switching of the clock pulses. Low power logic gates are used here by utilizing GDI technique. A new design of low power flip-flop is proposed which further accounts for power reduction. Simulations are done on tanner EDA 14.1 on 90nm technology. The proposed design shows 44% power reduction when compared to the design of Johnson counter using clock gating.

Keywords - Johnson counter, Clock gating, T-flip-flop, GDI technique

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I. INTRODUCTION

Earlier, the VLSI designers concentrated on the factors like area, performance, cost and reliability. Power performances were of the secondary importance. But now-a-days, as chip size is decreasing and many other micro-electronics reliabilities are developing gradually, low power design of any system has become priority. As the system feature size is decreasing gradually and frequency is increasing rapidly, power dissipation has become one of the primary concerns. A high operational frequency increases the power dissipation in the chip. Portable devices powered by batteries like mobile phones, laptop etc, have also influenced the need for power minimization in such systems

In certain computer applications, various arithmetic, logical and memory operations are performed synchronously with the clock. The sequential circuits in the system are the major contributor to the power dissipation as one of the inputs of the sequential circuits is the clock, which switches all the time. So, effective design of sequential circuit is very important for any computer system. Johnson counter is a sequential circuit which provides special kind of data sequences. It is the modification of the ring counter in which the inverted output from the last flip-flop is connected to the input of first flip-flop. It requires half the number of stages as compared to the ring counter.

Clock Gating technique is the most effective and popular technique for reducing the power dissipation in VLSI sequential circuits. It is used to eliminate the unnecessary switching of the clock in the Johnson Counter. Several researches have shown that clock power is major contributor (about 15-45%) of the power dissipation which is expected to increase in the coming years. This is due to the fact that power is directly proportional to voltage and the frequency of the clock as shown in the following equation:

$P=CV^2f$ where C is the capacitance, V is the voltage and f represents frequency

If we avoid the ineffective clock pulses in the system, then power can be appreciably minimized of any sequential circuit. Clock management system is plays a key role in sequential system.

In this paper, Johnson counter with clock gating is studied. This design has reduced power dissipation as compared to the conventional design but clock gating logic being additional circuitry has its own power dissipation. Here, a new Johnson counter is designed which has improved clock gating logic and thus, reduces power dissipation to appreciable amount.

In section II, the techniques used in the paper are described. In section III, the proposed design of the Johnson counter with clock gating logic along with proposed design of its various blocks is described. Section IV shows the simulation and results of the design.

II. TECHNIQUES USED IN THE DESIGN

In this paper, two low power techniques are used which give appreciable power reduction.

A. Clock Gating Technique

This is the most efficient method of reducing the power dissipation by suppressing the unnecessary switching of the clock. The

schematic of clock gating technique is shown in fig1.

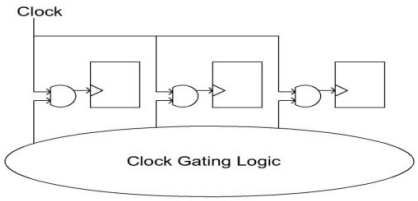

Fig1. A clock gating logic design

Clock gating logic is the technique in which the clock pulse is not provided when the output is same as the input. For the output bits Q1, Q2, Q3, Q4; bits toggle only on the two places in the complete cycle of eight clock pulses.

Table 1

Clock pulse	Q1	Q2	Q3	Q4
1	0	0	0	0
2	0	0	0	1
3	0	0	1	1
4	0	1	1	1
5	1	1	1	1
6	1	1	1	0
7	1	1	0	0
8	1	0	0	0

The truth table of the Johnson counter is shown as table1. When we see the table of the Johnson counter, we notice that the toggling of the output occurs at only two pulses from eight pulses on each flip-flop. This is wastage of power. Here, clock gating logic comes into picture which provides the clock when toggling is required otherwise clock remains in sleep state. For 4-bit system the relationships are as follows:

$$Clk_{Q0} = (Q_0 \oplus Q_3).Clk_{master}$$
$$Clk_{Q1} = (Q_1 \oplus Q_0).Clk_{master}$$
$$Clk_{Q2} = (Q_2 \oplus Q_1).Clk_{master}$$
$$Clk_{Q3} = (Q_3 \oplus Q_2).Clk_{master}$$

This relationship gives the logic which stops the clock if the condition is 'false' and if the condition is 'true', then the clock is supplied for switching of the bits. This logic though reduces the power of the design but it is a additional circuitry and so has its own power dissipation. So, the logic gates used in this logic are designed here using other technique named GDI technique.

GDI Function

A basic GDI cell is constituted of four terminals-G, P, N & D. The schematic is shown in the fig. G is the common gate of both the P & N transistors, N is the external diffusion node of NMOS transistor, P is the external diffusion node of PMOS transistor and D is the common drain of both the transistors. A basic cell is shown in fig. 2

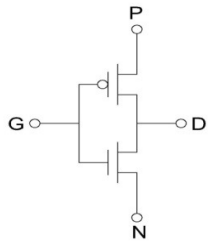

Fig2. A basic GDI cell

This GDI cell can perform various logic functions for different input configuration. When GDI based designs are compared with standard CMOS and pass transistor logic designs, it gives simpler gates, lowers the number of transistors used in any design and thereby, reduces power dissipation in many implementations. Using this technique, low power GDI based XOR & GDI based XNOR gates are designed.

Clock Gated Johnson Counter

Here, a Johnson Counter using clock gating is described. Traditionally, a 4-bit Johnson Counter consists of four flip-flops and the output of last flip-flop is inverted and feedback as input to the first flip-flop which differentiates it from the ring counters. When we refer to the truth table of the Johnson counter, a specific pattern is observed. A schematic of Johnson counter using clock gating is shown in fig 1. A Johnson counter is shown in which various logic gates are attached to the input and output of the flip-flops. The circuitry of the logic gates shown is referred to as the clock gating technique. But this logic irrespective of reducing the power of the overall design, adds some power of its own due to its own additional circuitry. So, new design

is proposed which overcomes the shortcomings of this design.

III. Proposed design

Here, a new design of Johnson counter is proposed which reduces the power dissipation to appreciable levels. Design of Johnson counter using clock gating consists of various blocks shown in fig1. consists of XOR, XNOR and NAND logic gates. Being a 4-bit counter, it has 4-flip flops. We are reducing the power at component level.

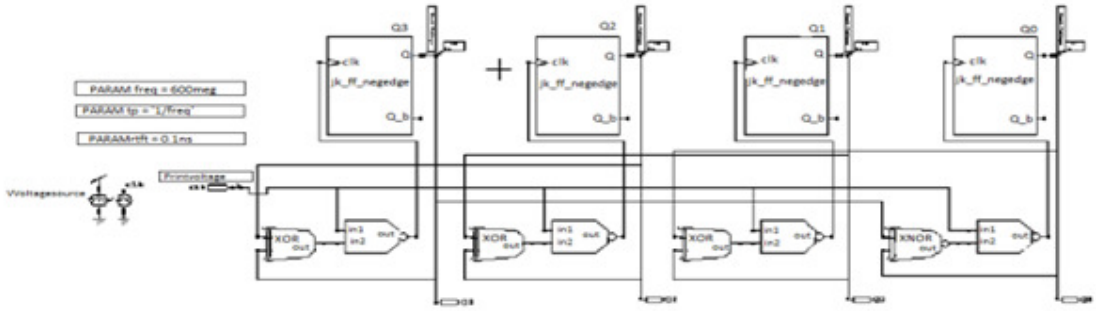

Fig 3: Design of Johnson Counter using clock gating

A. GDI based design of XOR- XNOR gate

When the input is '0' & '1', output of first inverter would be '1'. This '1' is provided to the bulk of nMOS. Bulk of pMOS has '0' and the output of the GDI cell is '1' which gives logic of XOR gate. This design uses less number of transistors as compared to conventional design so chip area is also reduced.

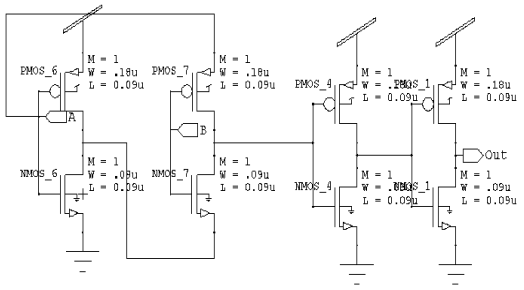

Fig4: Design of GDI XOR gate

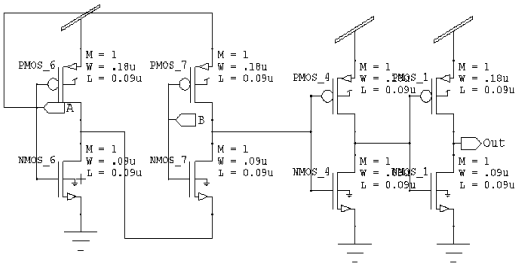

Fig5: Design of GDI XNOR gate

Power Comparisons

The power result for logic gates is shown in the table2. The power for the modified design is decreased in comparison to the conventional design.

Table2. Comparison of designs of XOR & XNOR gate

Frequency(MHz)	CMOS Xor (µW)	GDI Xor (µW)	CMOS Xnor (µW)	GDI Xnor (µW)
600	4.51	3.74	5.32	2.67
700	5.22	4.29	6.17	3.05

800	5.93	4.88	7.09	3.43
900	6.63	5.48	7.86	3.90
1000	7.31	6.06	8.71	4.39

The calculations are done for frequency ranging from 600MHz-1000 MHz.

B. Flip-flops

In the design of Johnson Counter [base paper], edge triggered flip-flop is used in master slave mode. The flip-flop used here are low power J-K flip-flop. As from the truth table 1, the output of last flip-flop is being inverted and given to the first flip-flop which shows that only toggling is being done. So, the flip-flop used here were in toggle mode and so the J & K terminals were always kept high in order to save power. This was a low power design but further optimization can be done. So, I have proposed a new design of flip-flop which shows more power reduction compared to conventional design. The schematic is given in the fig5.

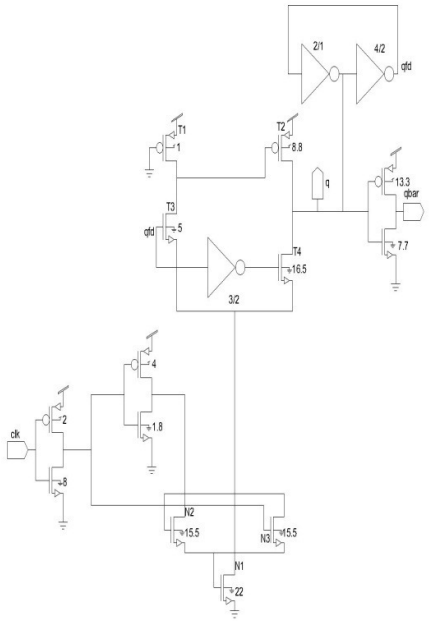

Fig6: Proposed Low power Design of T-Flip-flop

A two-input pass transistor logic (PTL) based AND gate is formed with transistor N2, in conjunction with an additional transistor N3 [13][14]. This PTL based AND gate controls the charging and discharging of the transistor N1. The output node is zero most of the times since the inputs to the AND logic are mostly complementary except during the transition edges of the clock. When both input signals equal to "1" (during the rising edges of the clock), temporary floating at node does not affect the output. A inverter is connected to the input terminal of the clock which delays the signal reaching at the two transistors N2 & N3. This inverted delayed clock controls the transistor N1. Both transistors turn on when falling edge of the clock is received which in result, turns on transistor N1 which discharges and charges the flip-flop.

In this design, a latch is connected which stores the output 'q' until clock edge is comes and transistor N1 is turned on. Transistor T1 is permanently on as it is ground which in turn which will turn off the transistor T2. When 'q'=0, 'qfd'=1, transistor T3 will be turned on and transistor T4 will be cutoff as the inverter will give output 0 which serves as input to transistor T4. So, the path comprising of transistor T1, T3 is closed through the charge will discharge through transistor N3. At this point, node 'P' will be high and as result will turn on transistor T2. Then output 'q'=1 and so, 'qfd'=0, transistor T3 is open and transistor T4 will turn on which closes the path on the connecting transistor T2 and T4 for discharging through transistor N1. Here, only toggling of the output is done and result is stored in latch to get accurate output.

Power Comparisons

The comparison of the power dissipation of the two flip-flops is shown on table. The proposed design of the flip-flop consumes almost half the power as compared to the conventional design of the edge triggered flip-flop in mater slave mode. The optimization done in the design of the flip-flop is thus verified.

Table3: Comparison of power consumption of the flip-flop

Frequency (MHz)	Average power consumption of flip flop used in different Design (µW)	
	Conventional	Modified

600	26.00	11.96
700	29.71	14.22
800	33.34	16.03
900	38.56	18.08
1000	44.15	20.84

IV. Proposed low power design of Johnson Counter

This is the proposed design of Johnson counter using clock gating which has effective power reduction as compared to basic Johnson counter using clock gating. The difference is in the designing of its various components that collectively make the clock gated Johnson counter. The proposed design consists of low power components such as proposed flip-flop is used here which accounts for huge power dissipation reduction. The GDI based XOR & XNOR logic gates are used which further contribute for power reduction.

Simulations

We have run simulations for our proposed design as well as for conventional clock gated design. We have also done simulations for conventional Johnson counter without clock gating for better comparison of the results. Here, all the simulations are done on 4-bit Johnson counter in conventional, clock gated and proposed clock gated Johnson counter. All the three simulations are analysed and compared for discussing the advantages of the proposed design. Fig8. shows the output waveforms of the 4-bit Johnson counter.

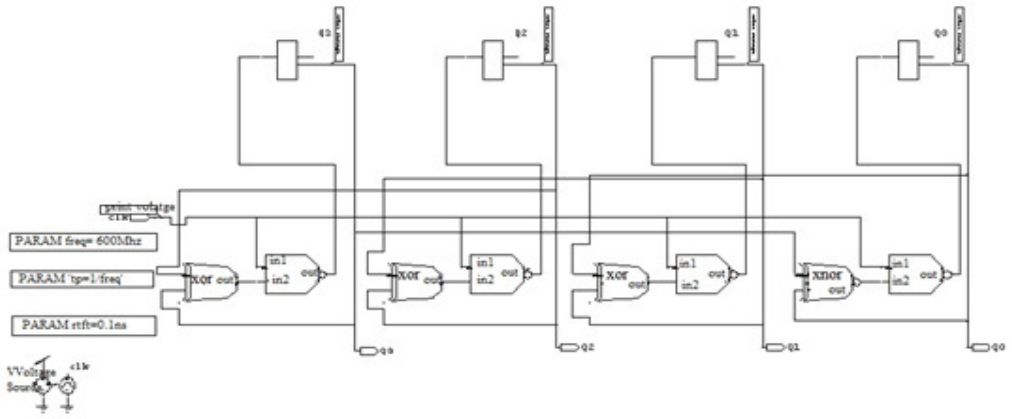

Fig7: Proposed design of Johnson counter using clock gating

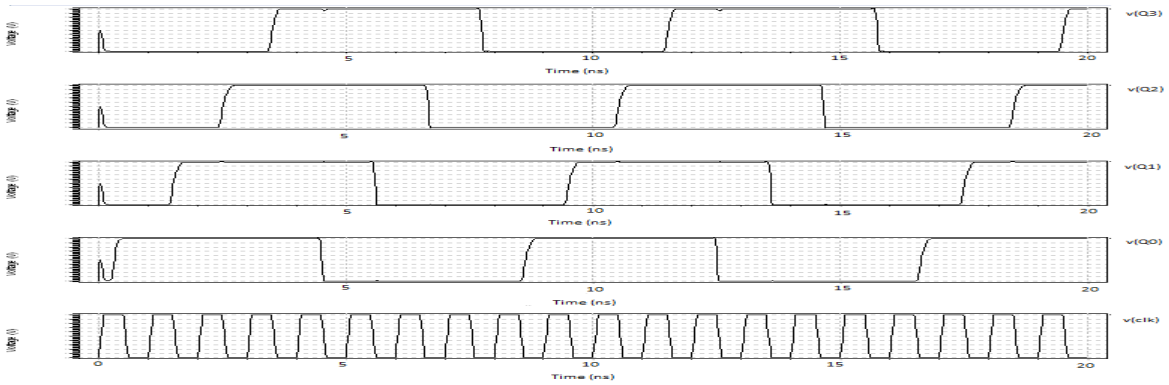

Fig8: Waveforms of Johnson counter

From the given simulation results, it can be seen that the proposed design is working on higher frequencies also which is not possible in clock gated design of Johnson counter. The power consumption of the proposed design is 66% approx less compared to the conventional Johnson counter and 44% approx less compared to the clock gated Johnson counter.

Table4: Power comparison of the three designs of Johnson counter

Frequency (MHz)	Design Average Power Consumption (µW)		
	Conventional	**Clock Gated**	**Proposed**
600	105.62	66.41	36.68
700	123.48	73.53	40.54
800	138.96	81.87	45.31
900	157.56	_	50.19
1000	171.91	_	54.69

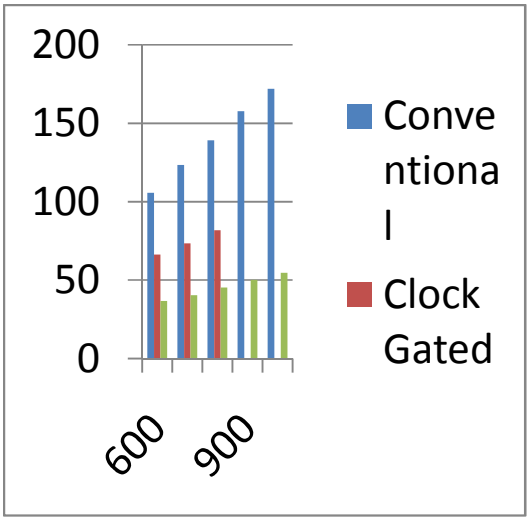

Fig9: Graph showing the power dissipation of the design

Table5: Comparison of three designs on the basis of various factors

Delay of the three designs(ns)				Number of transistors	
	Average Power(µW)	Delay(ns)	Power-Delay Product(pJ)	MOS in single flip flop	MOS in whole circuit
Conventional Design	138.96	0.164	0.022	34	144
Clock gated Design	81.87	0.345	0.028	34	214
Proposed design	45.31	0.267	0.0121	19	122

Conclusion

The proposed design shows reduction in the power dissipation. Due to the use of clock gating we have achieved a power reduction of 37.12% to 41.08% for different frequencies. Reduction of power ranges from 65.27% to 68.18% when proposed design is compared to conventional Johnson counter Design. The range of power reduction for proposed design compared to clock gated design is 44.76% to 44.65%.

