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Four-Leg Inverter Analysis for Minimizing the Common-Mode Voltage

Vidhun M
Assistant Professor
IES College of Engineering
vidhunveru@gmail.com

Pranav M S
Assistant Professor
IES College of Engineering
pranavms1@gmail.com

Josily Jose
Assistant Professor
IES College of Engineering
jose.josily@gmail.com

John J Thanikkal
Assistant Professor
IES College of Engineering
johnjthanikal@yahoo.co.uk

Abstract

An approach to reduce common-mode voltage (CMV) at the output of inverter using four-leg inverter is studied. A comparative study of three-leg and four-leg inverter is made for CMV reduction. The conventional three-phase three-leg inverters produce huge amount of common-mode (CM) voltage. The addition of a fourth leg to the bridge of a three phase inverter eliminates the common-mode voltage to ground created by the modulation of the inverter. An appropriate four phase LC filter is inserted between the inverter and the load in order to create sinusoidal output line-to-line voltage. The modulation strategy thereby completely eliminates the common-mode potential produced by traditional modulation techniques with traditional three-phase inverter topologies. A new switching control scheme called jump-edge delay is introduced in the four-leg inverter and compared with two other control methods to reduce the Common-mode voltage.

Index Terms

Common mode voltage, electromagnetic interference, four-leg inverter,Sinusoidal pulsewidth modulation

Nomenclature

i_{ds}, i_{qs}	d-q-axis stator currents in synchronous rotating frame.
v_d, v_q	d-q-axis stator voltages in synchronous rotating frame.
i_s	Stator current
M	Mutual inductance
i_{sra}, i_{srb}	Two phase components of rotor currents referred to stator
i_{sa}, i_{sb}	Two phase components of stator current
V_{sa}, V_{sb}	Two phase components of stator voltage
σ	Total leakage factor
T_e	Developed torque
R_s,R_r	Stator and rotor resistances referred to stator
L_s,L_r	Stator and rotor inductances referred to stator

I. Introduction

In a typical three-phase power inverter drives, there exists substantial common-mode voltage between the load neutral and earth ground. PWM inverters generate high frequency and high amplitude common mode voltages, which induces shaft voltages on the rotor side. When the induced shaft voltage exceeds the breakdown voltage of the lubricant in the bearings, it results in large bearing currentsThis causes premature failure of the motor bearings and also poses EMI issues.

Switching converters are used in electric drive applications to produce variable voltage, variable frequency supply which generates harmful large dv/dt and high-frequency common mode voltages (CMV) and Because of the unbalanced construction, the conventional three-phase three-leg inverters produce huge amount of common-mode (CM) voltage. It can ensure the output balance of four legs in inverter under any conditions reduces the generation of CM voltage. Four-leg inverters generate lower CMV as compared to conventional two-level inverters. In motor drives and electrical networks, common-mode current even has the potential to cause physical damage or unwanted tripping of ground fault relays. In typical three-phase power inverter drives, there exists substantial common-mode voltage between the load neutral and earth ground.

There exist several modulation schemes available in literature to eliminate common-mode voltage on load condition such as PWM, hysterisis,space vector[4][5] etc.. provided total sum of voltages in each leg should be zero and the load must be balanced.

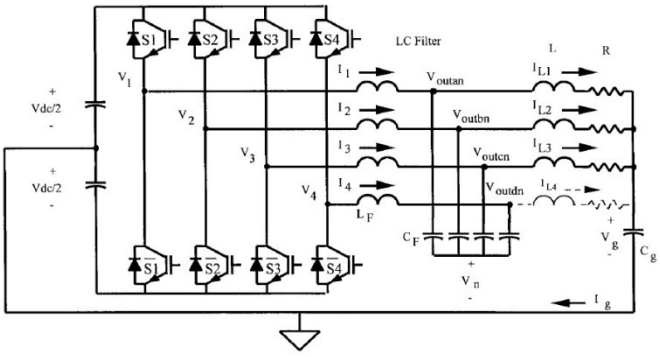

Fig. 1. Four-leg inverter with second-order filter and motor load[8]

The common mode voltage causes larger common-mode currents with increase in modulation frequency and decreases in machine zero sequence impedance worsening electromagnetic interference (EMI) problems and potentially damaging the network or the machine. A four leg inverter is used to reduce common-mode voltage as an alternative to expensive and large high-impedance common-mode filters. The four-leg

topology needs an additional pair of semiconductor Switches and a driver circuit. However, the fourth leg gives an additional degree of freedom to control and compensate the neutral current in a three-phase four-wire system.

II. The Three-Phase Three Leg Inverter

CM voltage of PWM inverter is defined as the potential difference from its output neutral to the ground. The CM voltage of a three-phase three-leg inverter[8] can be written in the form:

$$V_g = \frac{1}{(L_f + L)C_g s^2 + RC_g s + 3}(V_1 + V_2 + V_3) \quad (1)$$

where V_1, V_2 and V_3 is the output voltage of the inverter respectively; L_f and C_f is the filter inductor and capacitor respectively; L and R is the equivalent load inductor and resister of each phase in motor respectively; C_g is the equivalent CM capacitance of the motor. Because V_1,V_2 and V_3 equals nothing but $+V_d/2$ or $-V_d/2$, the state $V_1 + V_2 + V_3 = 0$ can not appear. Thus the CM voltage Vg always exists. The main cause of the CM interferences is the unbalance of the inverter's output voltage.

III. The Three-Phase four-Leg Inverter

In a four-leg inverter one more leg is added to solve the unbalance output voltage. The main requirement to reduce common mode voltage is that two top switches and two bottom switches should be on at all the time in order to satisfy the equation:

$$V_1 + V_2 + V_3 + V_4 = 0 \quad (2)$$

a sinusoidal PWM modulation, zero-state condition occurs and this zero-state ($V_1 = V_2 = V_3$)condition turns all the switches of all the bottom switches to turn on in the first three legs of the inverter. Due to this the condition(2) cannot be satisfied and CMV flows through the circuit. In order to reduce the effect of zero-state the modulation index should be less than 0.66. The best staggered time of the triangle carrier peaks is Tc/3 where Tc is the time period of the triangle carrier wave. In the four-leg inverter first three-leg switching is done by carrier phase shifting modulation and the fourth leg should be switched in the form:

$$S_4 = S_1 \oplus S_2 \oplus S_3 \quad (3)$$

where S_1, S_2, S_3 S_4 are the top switches of four-leg inverter. Actually the zero-state cannot be fully avoided by this method and therefore a small unbalancing will be created in the circuit which leads to a CMV, but it will be low compared to a three-leg inverter.

The situation can be improved a little if the fourth leg control is changed from exclusive-or(XOR) to threshold as follows.

$$S_4 = S_1 + S_2 + S_3, S_4 = \begin{cases} 0, & \text{if } S_4 \geq 2, \\ 1, & \text{if } S_4 < 2. \end{cases} \quad (4)$$

Threshold control reduces the common-mode voltage to a great extent compared to that of exclusive-or control.

IV. Theoretical Proof to Eliminate Common-Mode Voltage

Assume four phase balanced load for the calculation of CMV using four-leg inverter as shown in fig.1. The following differential equation is obtained from the fig.1

$$V_1 = sL_F I_1 + sLI_{L1} + RI_{L1} + V_g \quad (5)$$
$$V_2 = sL_F I_2 + sLI_{L2} + RI_{L2} + V_g \quad (6)$$
$$V_3 = sL_F I_2 + sLI_{L3} + RI_{L2} + V_g \quad (7)$$
$$V_4 = sL_F I_2 + sLI_{L4} + RI_{L2} + V_g \quad (8)$$

where s is the differential operator. The ground voltage is given by

$$V_g = \frac{I_g}{sC_g} \quad (9)$$

The current nodal equation is given by

$$I_{L1} + I_{L2} + I_{L3} + I_{L4} = I_1 + I_2 + I_3 + I_4 = I_g \quad (10)$$

Adding equations (5)-(8) and substituting in (9) and (10) gives

$$V_1 + V_2 + V_3 + V_4 = 0 = \left(sL + R + \frac{4}{sC_g}\right) I_g - sL_f \quad (11)$$

$$\Rightarrow I_g = 0 \quad (12)$$

from equation (9) V_g is also equal to zero. Also it is possible to show that filter neutral voltage V_n is also equal to zero.

Practically a four-phased load is not possible. A small unbalancing will be created in the circuit but it will not result much significant impact to common-mode voltage. The transfer function [6] of filter neutral voltage with respect to V_4 excluding the fourth phase load can be written as:

$$\frac{V_n}{V_4} = \frac{s^2 L_F + sR_F}{s^4 b_4 + s^3 b_3 + s^2 b_2 + s b_1 + b_o} \quad (13)$$

where L_f ,R_f are the filter resistance and inductance of the circuit.

The coefficients of this characteristic equation are:

$$b_4 = 4L_F C_F L + 3C_F L^2 \quad F \quad (14)$$
$$b_3 = 4RL_F C_F + 4R_F C_F L + 6R_F C_F L_F \quad (15)$$
$$b_2 = 12L_F \frac{C_F}{C_g} + 4R_F C_F R + 4(L_F + L) + 3C_F R^2 \quad F \quad (16)$$
$$b_1 = 12R_F \frac{C_F}{C_g} + 4(R_F + R) \quad (17)$$
$$b_o = \frac{}{C_g} \quad (18)$$

V. Improved Control Strategy

If the modulation index of sinusoidal PWM is reduced to a value less than 0.66, the utilization ratio of DC voltage will be reduced to a smaller value. Under the carrier phase-shift control, if modulation indexM_a > 0.66, the zero-state will appear near the sine wave peaks of each phase in four-leg inverter. The CM voltage will be enormous.

A. Jump Edge Delay Control

If the state of one leg (as Sc =1 in Fig.2) among the first three legs is reversed while the states of the other two legs (as S_1 and S_2) in Fig.2 are the same as the post-reversal state (as Sc = 0) of the being reversed leg, the state of the being reversed leg will be locked on the prereversal state (as Sc = 1) until one of the other two legs appears reversal. This method means that the jump edge of sinusoidal pulse width modulation(SPWM) is delayed when zero-state appears and zero-state can be avoided entirely. Thus, by using this control strategy, the CM voltage can be reduced largely in arbitrary modulation index. But the jump edge delay control will cut the SPWM pulse energy on the local waveform. So the total harmonic distortion of output voltage will get worse.

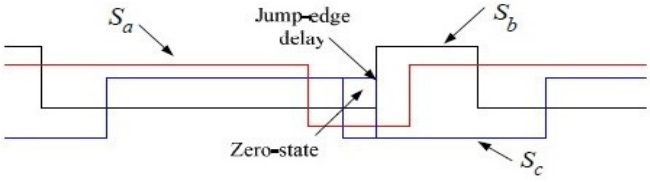

Fig. 2. Jump Edge Delay Control

VI. SIMULATION MODEL

The overall simulink model is shown in fig.3 and each block in the model is shown separately for the four-leg inverter. The simulink model of inverter and jump-edge delay control are shown in fig.4 and fig.5 respectively.

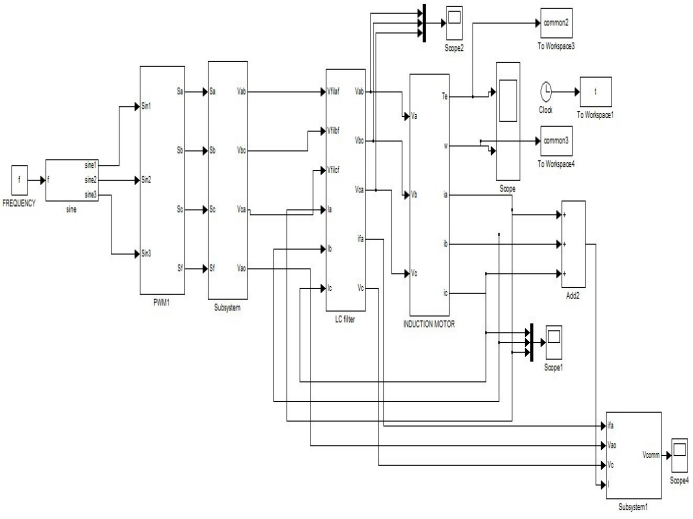

Fig. 3. Simulink Model

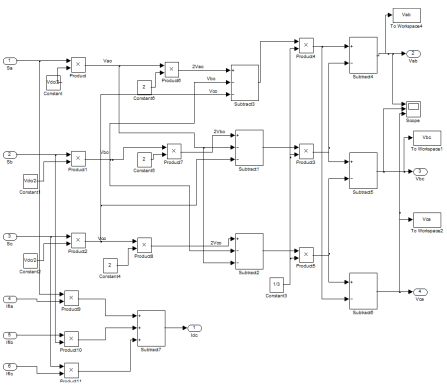

Fig. 4. Inverter Model

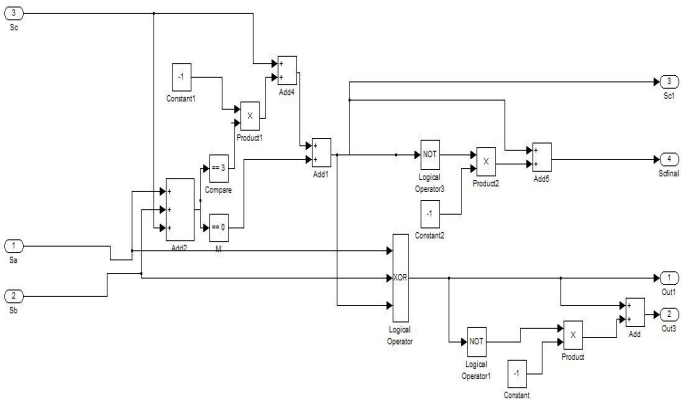

Fig. 5. Jump edge delay control

VII. SIMULATION RESULTS USING INDUCTION MACHINE AS LOAD

The minimization of common-mode voltage in induction machine using four-leg inverter is obtained about 1/4 times lower than that of three-leg inverter. As shown in fig.6 and fig.7 the common-mode voltage comes around 200V and using four-leg inverter the CMV comes around 50V. This shows that the CMV can be reduced to a certain level using four-leg inverter with suitable modulation scheme.

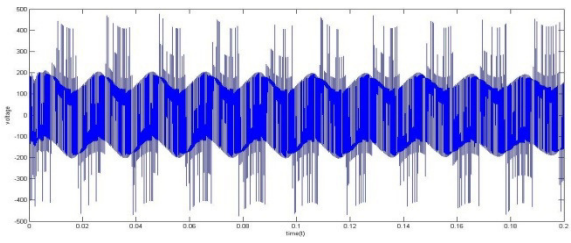

Fig. 6. Common-mode voltage of three leg inverter

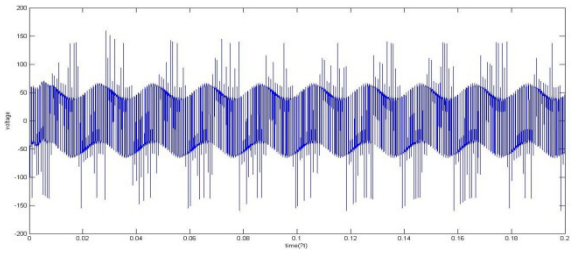

Fig. 7. Common-mode voltage of four-leg inverter

VIII. SIMULATION RESULTS USING RL AS LOAD

The CMV and the ground current is simulated using RL load. The fig.8 and fig.9 shows the CMV and ground current of three-leg inverter. The CMV comes around 300V and the ground current comes around 3A for three-leg inverter.

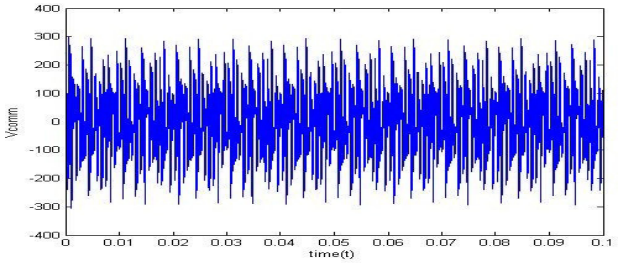

Fig. 8. Common-mode voltage of three-leg inverter

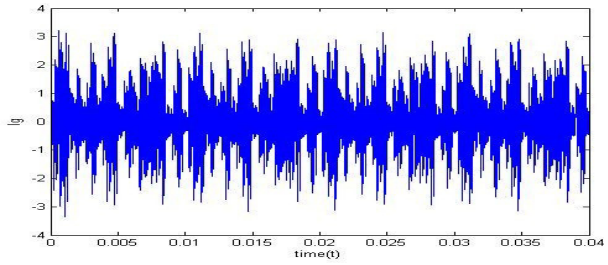

Fig. 9. Ground current of three-leg inverter

A. XOR control

The common-mode voltage and ground current obtained using XOR control of four-leg inverter is shown in fig.10 and fig.11. The CMV obtained is reduced to around 150V except certain peaks at 250V due to zero state. Similarly the ground current is reduced to 1.5V except few peaks at 3V due to zero state than that of three-leg inverter.

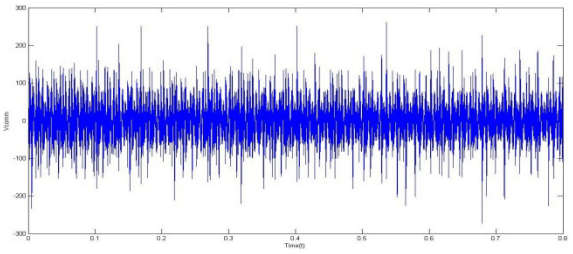

Fig. 10. Common mode voltage using XOR control for RL load

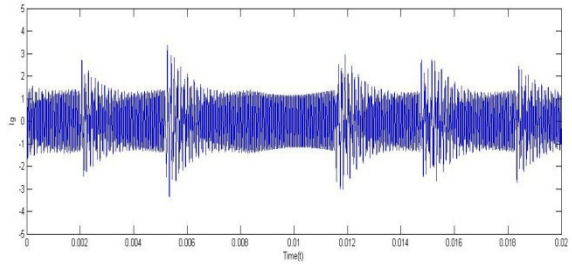

Fig. 11. Ground current using XOR control for RL load

B. Threshold Control

The common-mode voltage and ground current obtained using Threshold control of four-leg inverter is shown in fig.12 and fig.13. The CMV is reduced around 100V and the ground current is reduced below 1A except few peaks around 2A due to zero state than that of three-leg inverter.

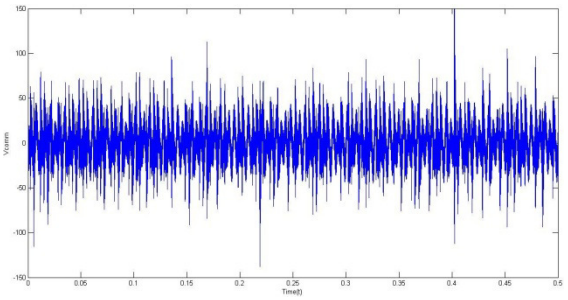

Fig. 12. Common-mode voltage using Threshold control for RL load

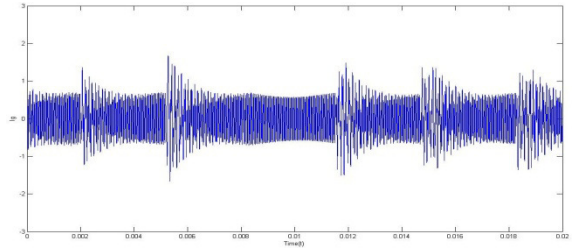

Fig. 13. Ground current using Threshold control for RL load

C. Jump-Edge Delay Control

The common-mode voltage and ground current obtained using jump-edge delay control of four-leg inverter is shown in fig.14 and fig.15. This type of modulation control is much better than other two modulation scheme in the manner it completely eliminates the zero state condition. It limits the CMV to about 50V and the ground current to 0.02A which is a very small value.

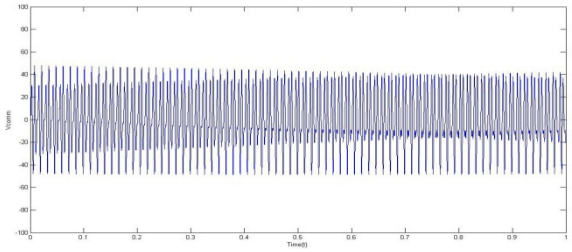

Fig. 14. common-mode voltage using Jump-Edge Delay Control for RL load

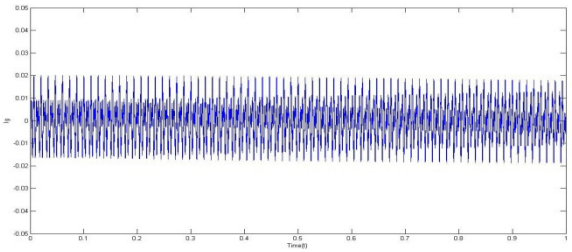

Fig. 15. Ground current using Jump-Edge Delay Control for RL load

IX. Conclusion

The three phase four-leg inverter greatly reduces the common-mode voltage compared to traditional three phase three-leg inverter. Different types of modulation schemes for four-leg inverter were used such as XOR, threshold control and jump delay control out of which jump delay control modulation were very effective to reduce common-mode voltage and ground current.

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