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Delay Improved 4-bit Multiplier using Pyramidal Adder

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Abstract- Improving the performance of digital adder is needed as they are widely used in FPGA based VLSI environment and DSP Processor operations.Binary multiplier basically madeup of rearrangement of adders and so multipliers completely depends on adders. Adder plays vital role in DSP processing applications and FPGA based VLSI environment where power,delay,speed and area are important parameters,so we need to reduce all parameter values as possible as possible.Power,delay,speed and area all are important values and are depend on multiplier which in turn depends on adders.So if we modify the adders namely half adder and full adder we can reduce required parameter values.By implementing nomal half adder and full adder we can reduce the delay.

Keywords- digital signal processing (DSP), multiplexer (MUX), half adder (HA), full adder (FA), and field programmble gate aray (FPGA).

I. INTRODUCTION

Multiplication of two bits carried out by completely with adders, multiplication includes generation of partial products, adding of partial products, methods such as parallel computing of partial products and carry propagating, all these approches are implemented with combinational devices.

In arithmetic operations addition is the major operation to perform arithmetic operations like multiplication, subtracting,dividing ,comparing and finding a square root.In multiplication operation , addition is the basic operation to find multiplication of two binary bits.Addition plays crucial rule in DSP processor applications,in FPGA based binary multipliers and in computer application In all applications power,dealy and area requirement all are depend on multipliers which in turn depends on adders.

Binary half adder is hardware formed complex circuit with five logic elements ,if we use such half adder in mullti-combinational adders it gives more complex circuit for example for 1024-bit DSP processor,and also speed is reduced due to serial connecting logic elements .For nxn bit multiplier, nxn AND gates and n (n-1) OR gates are required, in terms of adders n half adders and n(n-1) full adderes are required. Improving the performance of digital adder is needed because execution of binary operation completely depends on adders, there are so many adders are implemented such that to meet the requirements of FPGA based VLSI environment and DSP Processor operations.

Ripple carry adder: It is simplest adder among all adders but slowest adder, it requires o(n) and delay of o(n),where n represent the operand size

Carry look ahead adder: It has good area o(nlogn) and good delay of o(logn),but suffers from irregular layout design

Carry select adder: It has area of o(n) and delay with $o(n^{l+2/l+1})$,and it is the best adder in terms of area and delay

Carry save adder: Requires area o(n) and delay of o(logn)

Carry select adder is ths fast adder as it reduces computation time for operation among all adders but suffers from fanout limitation.The sorting problem is defined as the rearrangement of N input values so that they are in ascending order, merge sort method uses divide and conquer algorithm and uses recursion to perform sorting.

2. EXISTING METHOD

Hardware complexity of multipliers can be geatly reduced by using so many hardware structures and in those one of the structure is pyramidal adder. The Structure of 4x4 bit multiplier using pyramidal adder which consists of inputs $a_3,a_2,a_1,a_0,b_3,b_2,b_0,b_1$ whose partial products are given to four

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3x3 bit pyramidal adders with 2.1 and 2.2 blocks which acts as half adders used in the place of full adders and half adders.

Sorting is one of the common problems of data processing and is generally understood as a problem of placing elements of disordered set of values of data sets in order of monotonic increase or decrease. Using specialized equipment gives an ability to perform with high efficiency sorting operation of a given algorithm in relation to the universal computer system. There is a significant number of known algorithms for sequential and parallel sorting data sets that can be implemented in hardware

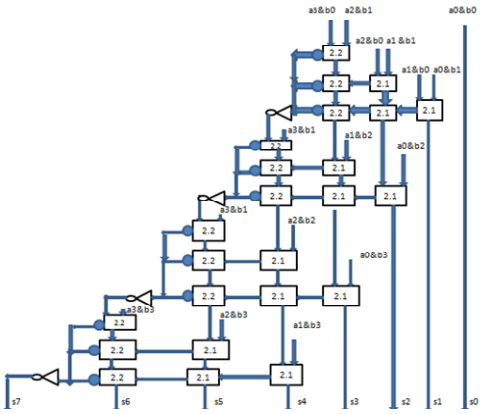

Figure (1): 4-bit multiplier with Pyramidal adder

The structure of 3x3 bit pyramidal adder is shown below,that performs the addition of three two input bits and generates the four outputs. In 4x4 bit multiplier the partial products are given to 2.2 and 2.1 blocks of 3x3 pyramidal adders. One 3x3 pyramidal adder can generate three sum outputs and final carry output by using three 2.1 and three 2.2 blocks.

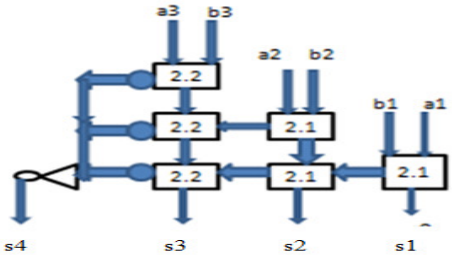

Figure (2): 3-bit Pyramidal adder

It contains single input 2n bit bus carrying inputs (a_0b_0, a_1b_1 a_2b_2 a_3b_3…..a_nb_n),the pyramidal structures contains three single bit aders namely 2.1 block to direct transfer of outputs,2.3 block to transfer inverse outputs,and 2.3 block to inverter the output bus of combinary adder (S_0 S_0,$S_1S_2S_3$…..S_7),here 2.1 and 2.2 blocks acts as half adders as compared to half adder with five logic gates ,so there is a reduction of gate count in the mulipliers with 2.1 and 2.2 blocks.if binary braun multiplier is implemented with pyramidal adder the gate count is reduceed and speed of operation also increased.

2.1 block (normal Half Adder)

It uses NAND gate, AND gate and OR gate, its function is

$S_i=(a_ixb_i)x\ (a_i+b_i)= =a_i\ 'xb_i+a_ib_i'$

$P_+= a_ixb_i$

Where S_i is the sum and P_+ is the carry

2.2 block (normal Full Adder)

It uses two NAND gates and one OR gate

It uses NAND gate, AND gate and OR gate, its function is

$S_i= (a_ixb_i)'x\ (a_i+b_i) = a_i\ 'xb_i+a_ib_i'$

$P_+= (a_ixb_i)'$

The P_+ is given to inverter to get final carry P_+

To generate s_0 and c_0, one 2.1 block is required. To generate S_1 two 2.1 blocks will be required and carries c_1 and c_2 will be generated from each block along with s_1. To generate S_2 three 2.1 blocks will be required and carries c_3, c_4, c_5 are generated. To generate S_3 four 2.1 blocks will be required and carries c_6, c_7, c_8, c_9 are generated from each block and so on. To generate the S_{15} Fifteen 2.2 gates are required and carries c_{105}, c_{106}….c_{119} are generated from each block. All these carries are multiplied and given to the inverter to generate the final carry out. Thus all the sums and carry are generated using the pyramidal adder. This adder performs addition with minimum delay when compared to normal adders.

For standard 4x4 bit Braun multiplier using half adders and full adders consists there are 120 gates if multiplier is implemented with pyramidal adder the gate count is 76.

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3. IMPLEMENTATION OF PYRAMIDAL ADDER WITH XNOR AND MUX

Standard adder which uses normal half adders and full adders.Figure (a) and (b) below shows normal half adder and full adder which uses NAND and OR gates.For Pyramidal adder modified half adder and full adders are implemented with XNOR and MUX with that both gate count and delay is reduced compared to standard adder.In Figure (3), Fig(c) and Fig (d) shows the modified half adder and modified full adder.

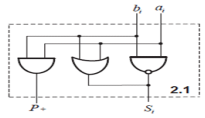


Fig.(a):Normal Half Adder

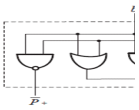


Fig.(b):Normal Full Adder

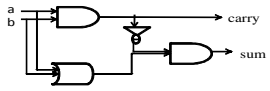


Fig.(c):Modified Half Adder

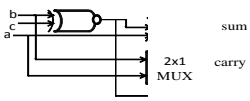


Fig.(d):Modified Full Adder

Figure (3): Normal and Modified Half Adder and Full Adder

Here 2.1 block and 2.2 blocks acts as half adders hence ech block generates one sum and one carry bit

Modified Half Adder

Let a and b be the inputs and sum and carry are the outputs

Sum=(a&b)'x(a+b)

=(a'+b')x(a+b)……using demorgans law

=(axa')+(a'xb)+(bxb')+(axb')

=a'xb+axb'

=a^b

Carry=(a&b)

=axb

Here this modified half adder acts as normal adder with less number of gates, so my using this modified half adder the gate count can be reduced.

Modified Full Adder

Let a, b and c are the inputs and sum & carry are the outputs of modified full adder

Sum=(bXNORc)XNORa

=(b'c'+bc)XNORa

=(b'c'+bc)a'+(b'c'+bc)a

=(b'c')(bc)'a'+ (b'c'+bc)a

=[(b')'+(c')']]b'+c']a'+(b'c'+bc)a

=[b+c][b'+c']a'+(b'c'+bc)a

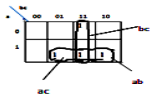
=[bb'+bc'+b'c+cc']a'+(b'c'+bc)a

=[bc'+b'c]a'+(b'c'+bc)a

=a^b^c

Carry=[b'c'=bc]b+[b'c'+bc]'a

=[b'c'+bc]b+[b'c+bc']a



=bc+ab'c+abc'

=(a+a')bc+ab'c+abc'

By using map

Carry=ab+ac+bc

Here modified full adder sum and carry values are same as normal full adder but topology isdifferent.The use XNOR's and MUX delay is reduced, as the MUX function is select to select output among inputs.

To generate S_0 no gate is required and to generate S_1 one half adder and one full adder required,partial products are given to adders to generate S_1 and two carries C_1 and C_2 respectievely.To generate S_3 one half adder and two full adders are used and generates carries C_3,C_4,and C_5 ,and as the partial product increases number of half adder and full adders also increases,here with modified half adder and full adder the outputs are obtained with minimum delay.

4. SIMULATION RESULTS OF 4-BIT MULTIPLIER USING PYRAMIDAL ADDER

16x16-bit pyramidal adder is designed and implemented xilinx ISE software and simulation res ults are verified.

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Fig. (a): Block diagram of 4x4 bit multiplier using pyramidal adder

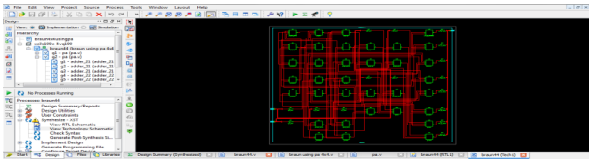

Fig.(b): Technology schematic of 4x4 bit multiplier using pyramidal adder

Figure (4): RTL analysis of 4-bit multiplier using Pyramidal adder

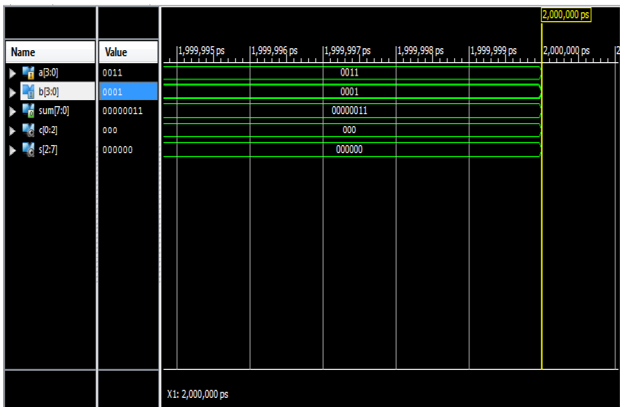

Figure (5): Simulation results of 4-bit multiplier using Pyramidal adder

5. CONCLUSION

Digital adder is widely used in FPGA based VLSI environment and DSP Processor operations.Binary multiplier basically made up of rearrangement of adders and so multipliers completely depends on adders .Binary multipliers are widely used in DSP processors and FPGA based VLSI domain environvment,where area,power,speed and delay are important parameters.All are can be controlled by implementing adders,there are so many adder structures are there for binary multipliers .pyramidal addrer is the one structure to reduce hardware complexity and delay.In this thesis normal half adder and full adders are modified with XNOR gates and MUX results minimum delay for 16 –bit pyramidal adders.

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