International Journal of Scientific Research and Engineering Development-– Volume 4 Issue 1, Jan-Feb 2021

Available at www.ijsred.com

RESEARCH ARTICLE OPEN ACCESS

Embedded applications focused on JTAG Interface on Fault Injection Technology

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Abstract:

The injection and testing of faults is an integral PHM form. With the architectures and functions of PHM and integrated modular avionics systems, defective injection often becomes more complex and traditional "PLUG, sample and adaptation plate" methods are difficult to use (IMA). Engineering systems also provide a software-based fault injection to monitor and operation bottle. This research aims to solve the problem of using software defect injections to validate testing through an error injection mechanism based on the interface of the Joint Test Action Group (JTAG). The technique is based on research parameters and takes the modularization and integration patterns of avionics into account and takes into consideration aspects of JTAG border scanning technology. Hardware defects can be injected in a non-contact manner using boundary scanning techniques and chip debugging. The exact and manageable defects of embedded chips/functions which meet simulation error and effect/time requirements can then be achieved. Thus it is possible to tackle problems with equipment-based injection defect architecture systems and to check new airborne PHM tests and integrated aeroplane testing equipment so that test index and PHM functions effectively help and ensure performance.

Keywords —Fault injection; PHM/testability verification; JTAG(Joint Test Action Group)

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Introduction

The injection failure is an effective method for validating PHM. However, with very broad integrated integration application, integrated system (VLSI) and high frequency/high-speed circuit boards are far higher. On the other hand, software-controlled injection errors are also not closely related to bottleneck problems, other fault injection problems such as chip packaging, circuit level integration and signal frequency. Normally, software defect injection efficiency is achieved by manually adjusting the code in question, but no

universal or formal requirements are available and would more likely influence the man-made factors. These variables make the output of software injections more difficult.

Its aim, through the proposal of the fault injection technology based on the JTAG interface, is to solve problems associated with the use of software failure injection for validation testing by taking into account advances of modularization and integration in avionics and incorporating JTAG border-scan technology aspects. Hardware malfunction injection can be done using border scanning technology and chip debugging functions. Injection failure of the chip pins/functions that meet injection effect/time and fault simulatory requirements is accurate and controllable. The main objective of this research is to address the issue of FPGA, DSP, ARM, PowerPC and High-Speed Circuit Boards such as VME and RapidIO simulators. Boards are available. Boards are available. Boards are available. Boards are available. The avionics device failure solution is based on a common and standardised platforms IEEE1-149,1 and JTAG interface. The software is fitted with BIT, Power-up-BIT and Initiated BIT. The JTAG port is ideal for setting, regulating and injecting a sequence of the chip's signal output frequency and for injecting and tracking an embedded chip failure in real time.

Literature Survey

JTAG software debugging devices are now among the most popular electronic devices, programmable chips like FPGA, PowerPC and DSP. So the concept of JTAG debugging may be used to insert a software error if the hardware cannot be handles or not tracked.Simulation of an internal high speed bus, for example by testing the built-in chip and its related control logic, failed simultaneously.The key to injection failure is therefore regulating and simulating faults for chip pin logic and device functions for embedded software and internal buses. In order to verify the integrated chip pins and monitor them, the IEEE1049,x series JTAG standards is used to control and detect the device in the software view. The test lines of IEEE1149.X actually occupy the lines of IEEE1149.1-2001; IEEE1149.4-2010, IEEE1149.51995, IEEE1149.6-2003. IEEE1149.1 is the most frequently used and generally recognised standard on all IEEE1149.1 circuits. IEEE1149.1 for determining injection digital circuitry technology of device faults is the key basis of this research. The boundary scanning technology of IEEE1149.2 involves a shift registry stage (in a boundary registry cell where symbols can be detected and monitored in scanning principles on component borders) adjacent to the pin component [1-5], [8]. The types of change records from IC to I/O pins are referred to as small scan cells and the BSC scan register is referred to

by the border scan registry (BSR). These registers are used during the test to track the status of the input pin (high or low) and to play the output pin and then to control the state of the unit and connections of the circuit board. Such additional changes do not impact the regular position of the circuit board in normal operation. The BSC is put at the limit of the chip by borderline scanning core technology, which provides the standard chip, the circuitboard and a test system for the serial setup and measurement of the state of the chip pins. In the IEEE 1149.1 standard you define the basic border-scan structure. Avionics systems use standards similar to IEEE for safety critical software verification [6],[7].

Implementation

A precise I/O operation with a strict timeline is appropriate for the purpose of this analysis. There are currently a range of supporting resources available for borde scans such as ScanWorks but the testing technical requirements like ASSET InterTech (Richardson, T XX, USA) and XJTAG are not entirely fulfilled (XJTAG Ltd., Cambridge, UK). This is a control procedure which differs radically from conventional single board testing. However, an IEEE1149.1 boundary scanning mechanism can be used for the scanning devices at business boundaries to provide the basis for the advancement of defect injection technology. The usage and cost efficiency of border scanning devices are also increased with the goal of providing a versatile API.

The JTAG scan chain architecture can be easily implemented if appropriate by selecting the boundary scanning framework that can provide an API. Figure 1 shows the JTAG border-scan technique of I/O power.

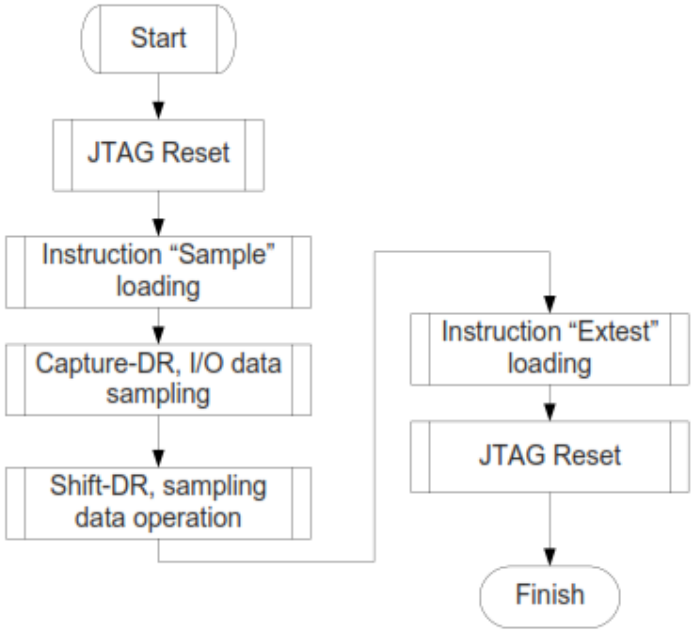

Figure 1. Schedule of I/O control based on the JTAG boundary-scan technique.

Software fault injection for embedded chips is shown in Fig. 2. As shown in Figure 3, a fault injection system can be designed in accordance with the technical implementation process. The device is XJLink2 which provides a standard benchmark structure for the PC and the J Target

Chip interface, and transforms control programmes on the PC into jtag pin timing that meets the IEE1149.1 specifications for connected scan chip border chain. The XJLink2 transfers control data to the scanning chain for the target chip, collects and transfers output information on the destination chip to your PC. XJLink2 handles the fault injection device's hardware architecture while configuring the injection mechanism PC's fault injector control programme.

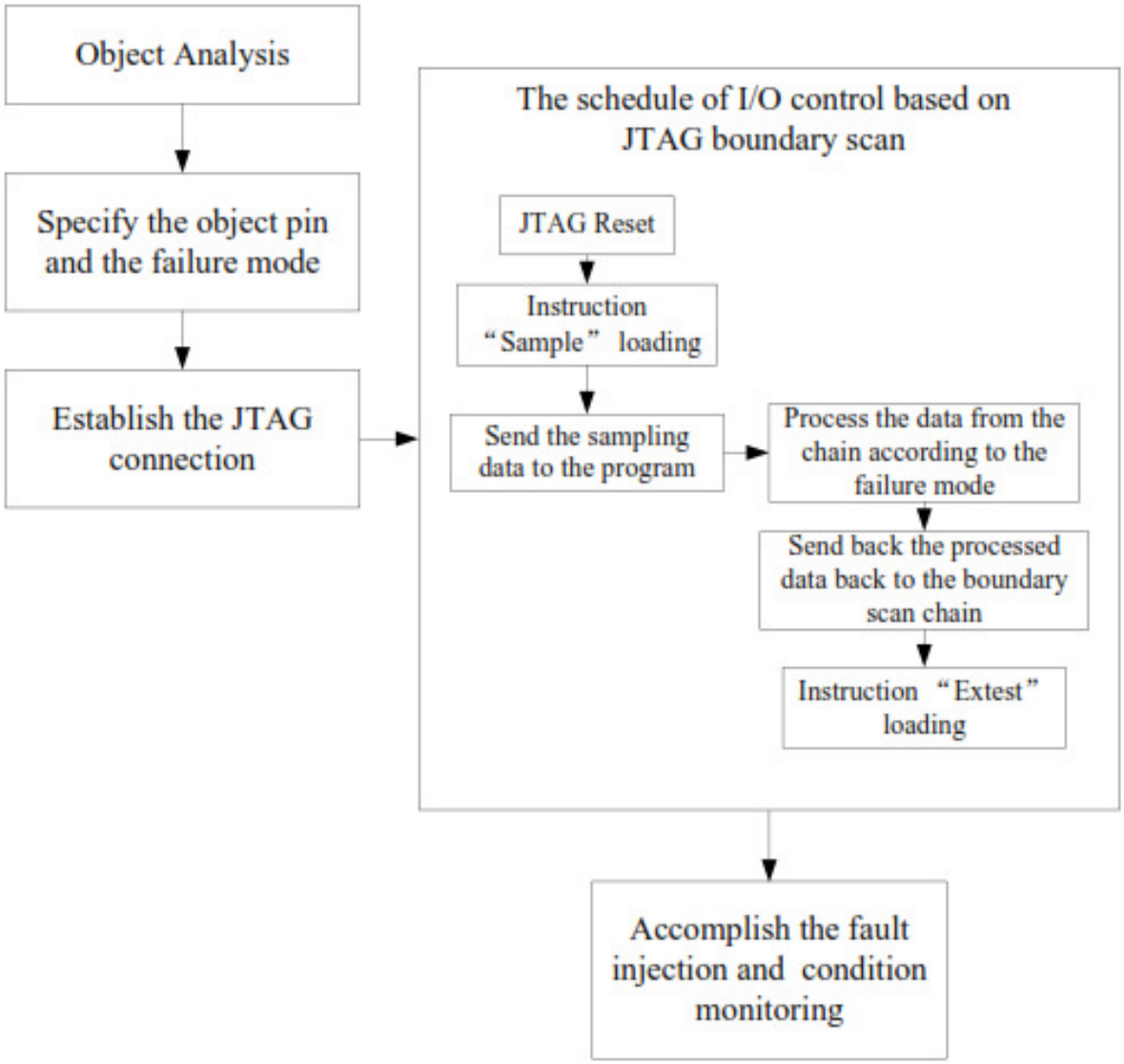

Figure 2.Software fault injection forembedded chips.

The software ensures the target computer and PC is connected to each other and collects the returned I/O information from the XJLink2 chip chain. Afterwards, the changed data are passed to the limit chain, and the information in the output pin generates the defect signal for the injection. We are digitally using DSP, Model No. 32-bit. Texas Instruments (Dallas, TX, USA). The TMS320F2812 borderline scan chain is an example of the technology scheme mentioned in this paper.

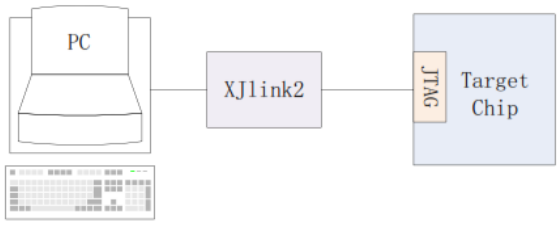

Figure 3.Architecture of fault injection system

The BSCs BC and BC4 IEEE1149.1 are the key componentes of the board. Figures 4 and 5 display block diagrams for both. The type BC 1 can be used only for the input pins or for the sample data and cannot track the output signal or affect the cellular structure of the BC 4 pins. The input or output pins of BC 1 are used. BC 1 and BC 4 have their attributes 1. Therefore, under the scheme defined here, the sample and tests of the BC 1 cell's output pin (or two-direction pin output status). For investigative tests, failure injection usually requires the correct control of the output pin properties and thus satisfies the requirements for fault injection as outlined in the paper.

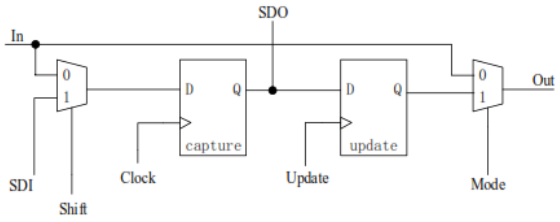

Figure 4. Standard boundary-scan cell BC_1

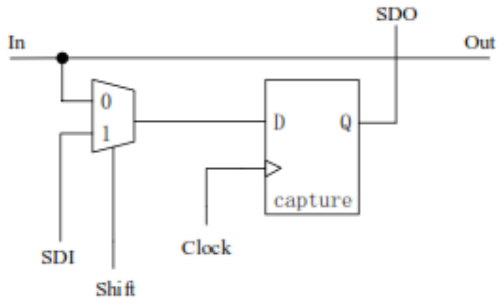

Figure 5.Standard boundary-scan cell BC_4

Conclusion

The paper is used to solve faulty simulation issues when testing the hardware when embedded software on JTAG interface is not operational or functional. A device failure injector of the programmable chip can be achieved in the FPGA standard unified platform based on IEEE1149.1 and JTAG interface debug mode. Included in the failure mode of technology simulation short runs, bridges, 1/0 pads, and open or closed conditions of a specific system (e.g. timer output, communication unit, interference, etc)

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