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Design of delay cell for VCO which provides good Figure of Merit of -189dBc/Hz and Phase Noise of -119dBc/Hz

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Abstract:

The major part of designing a VCO is to design a delay cell that provides the delay for VCO to oscillate. In our work, a delay cell or a delay unit is designed to obtain a tuning range which is wider and with good performance parameters in the first phase the delay cell is designed to oscillate in the desired oscillating frequency, and performance parameters are measured. In the second phase, additional techniques are used for improving the performance parameters of the VCO. A 45nm technology node is used to design the delay cell and VCO. Through this work, a low phase noise of -111dBc/Hz and a good figure of merit (FOM) of -190dBc/Hz is achieved.

Keywords **—VCO, Phase Noise, Figure of Merit, Delay cell.**

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I. INTRODUCTION

Unmanned aerial vehicles (UAVs), commonly referred to as drones, are air traveling vehicles that don't carry crew members on board and are instead flown remotely by humans, pre-programmed software, using Artificial intelligence, or both. UAVs come in a very wide range of sizes and payload capacities and are growing as semiconductor technology is shrinking every year. Drones in recent times are used for a variety of purposes, including cartography and mapping, police surveillance, delivery services, telecommunications relay, traffic monitoring, border patrol and reconnaissance, emergency and disaster monitoring, remote power line, and pipeline inspection, their use has grown exponentially over the past ten years. UAVs, which can be operated remotely and can be operated from very large distances these drones are typically utilized to operate in perilous or hostile countries without putting the operators in danger.These UAVs can be modified to carry a payload of a few kilograms. Because of affordability, simplicity to fly, and smaller size makes the detection of these UAVs very difficult. These UAVs if go into the hands of antisocial elements then there is a threat to the security of the country and its people so there is a need for designing radars that can detect and intercept these UAVs. Radar should be designed to detect drones of all sizes and from close proximity so that necessary actions can be taken to avoid the threats caused by these rough drones. A radar is basically an electromagnetic sensor, which is used to track and locate different objects from a wide range of distances. Radar basically transmits an electromagnetic wave in the direction of targets and observes the echoes. The major component used for the generation of this electromagnetic wave is the Local oscillator which generates a wide range of frequencies. a wide range of frequencies is achieved by varying the voltage so a VCO is used as a local oscillator in most of the radars

II. PROPOSED DELAY CELL

A differential pair can be used as a delay cell as it cancels out the input noise and has a good signal-to-noise ratio compared to the single-stage inverter. The output resistance of the differential pair is r01//r05 and the resistance r0 value depends on the current flowing through the transistors M1 and M5, which can be varied using control voltage Vc1 through tail transistor M6, for higher resistance at the output, a lesser current should flow through the transistors, similarly for lower resistance current flowing through transistors should be higher. Since the frequency of the oscillator depends on the resistance of the delay cell, we should be able to generate a wide range of resistance using the control voltage Vc1.differential pair used here offers a very good signal-to-noise ratio so a differential style of delay cell should be designed to obtain a good noise performance. the resistance and capacitance generated by conventional differential pair is very less for generating the desired range of frequency, so an alternative technique is to be used to generate this frequency range.

A cross-coupled differential pair can be used to increase the delay. Instead of using a fixed bias voltage for the PMOS transistors, a variable voltage can be provided for these transistors by connecting the output of the previous stage to the PMOS transistors of the current stage. the bias voltage of the PMOS transistors is varied by the previous stage output voltage thereby varying the resistance of the delay cell. By using a cross-coupled differential pair a better range of tuning range can be obtained when compared with the conventional difference pair. but not suitable to obtain the desired range of frequency. The delay of the cell can also be varied by changing the charging and discharging time of the delay cell thereby varying the frequency of the oscillator. A voltage-dependent frequency tuning can be achieved by using additional transistors to increase the charging and discharging time of the delay cell.

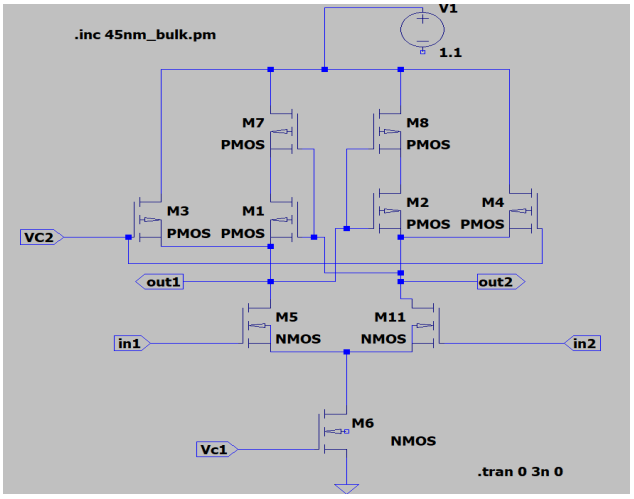

Fig.1 Proposed Delay Cell

The transistors M3 and M4 are used to enhance the output of each cell thereby providing a good signal amplitude which is an important performance parameter of the VCO.in this differential pair two control voltages Vc1 and Vc2 are used to generate the frequency tuning. Vc1 is used to control the bias voltage of the tail transistor M6 and Vc2 is used to control the gate voltages of the M3 and M4 transistors. Usually, one of the control voltages is fixed and the other control voltage is varied in VCOs with two different control voltages. During the charging phase, the transistors M1 and M3 are on and transistor M5 is off so based on the control voltage given to the gate of M3 and the voltage across the M1 transistor the charging time of the delay cell can be varied similarly the discharging path is through the transistors M5 and M6, by varying the control voltage across tail transistor M6 the discharging time can also be varied. The sum of charging and discharging time is the total delay of the cell, so the parasitics and size of transistors are selected to obtain the desired tuning range. The control voltages can be selected based on the required frequency and tuning range can be achieved.

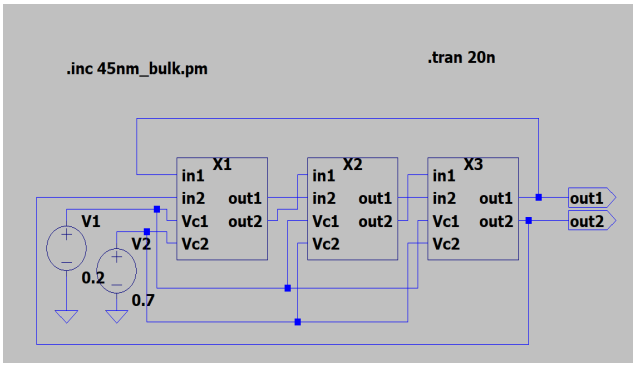

Fig.2*3-Stage VCO using designed delay cell*

This differential pair suffers from supply voltage variations and noise is induced into the cell thereby affecting the phase noise performance of the cell. There is a need for a technique that can reduce the noise induced because of supply voltage variations and results in a good phase noise performance. we know that cascading the transistors will reduce the supply voltage variations which helps in reducing the noise in the circuit. but the major disadvantage of using cascaded transistors is that it limits the swing of the transistors thereby the amplitude of the oscillating signal.

III. SIMULATION RESULTS

Two control voltages are used in this design and to achieve a maximum frequency, the delay of each delay cell should very small so control voltages are set at values of 0.7(VC1) and 0.4(Vc2) which charges the load capacitance very quickly there by reducing the delay, which resulted in a frequency of 18GHz.

the control voltages Vc1 at 0.2 and Vc2 at 1.1 makes the discharging time of the load capacitor higher by making the resistance offered by the delay cell higher. The resistance offered by delay cell with this control voltages is higher because, with a bias voltage of 0.2V the tail transistor M6 is not turned ON but because of sub threshold leakage current the load capacitance starts discharging slowly making the delay offered by the delay cell very high. A higher delay in the delay cell results in lower frequency. The main purpose of this design is to generate wide range of frequencies which are highly linear. sothe tuning of these frequencies should be varied linearly with respect to the control voltage.

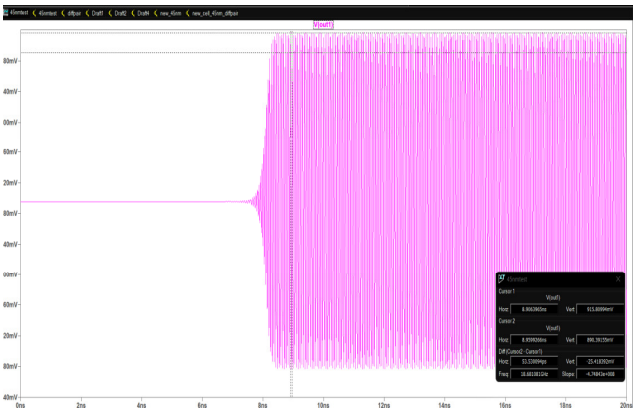

Fig.3*VCO oscillating at 18GHz*

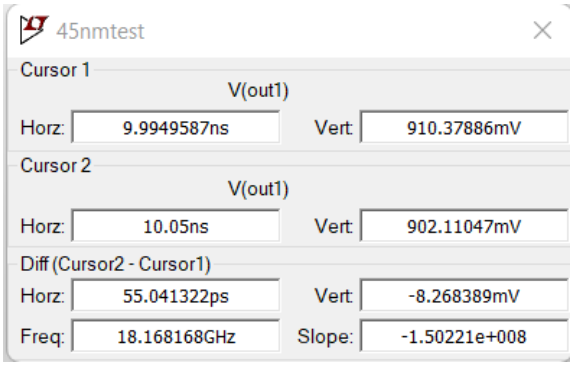

Fig.4oscillating frequency

Another important performance parameter of VCO is phase noise. Which is defined as the fluctuations in the signal phase with respect to the variations in the periodicity of the signal there are two major types of noise which affects the transistors, flicker noise and white noise or gaussian noise flicker noise at higher frequencies is dominant and at lower frequencies, white noise is dominant since we are designing the VCO for a wide range of frequency we should consider both the types of noise and their effect on the performance of the delay cell.the supply voltage variations also cause phase noise which affects the figure of merit, this issue of noise induction because of supply voltage variations is reduced by using a cascaded structure in the delay cell. A differential pair configuration also helps on reduction of noise so it is used in the design of the delay cell. phase noise variation with respect to the

frequency is shown in figure 5.phase noise and FOM of the designed cell are measured using the following formula.

$$FOM = -20log\left(\frac{fosc}{\Delta f}\right) + 10log\left(\frac{pdc}{1mw}\right) + L(\Delta f)$$

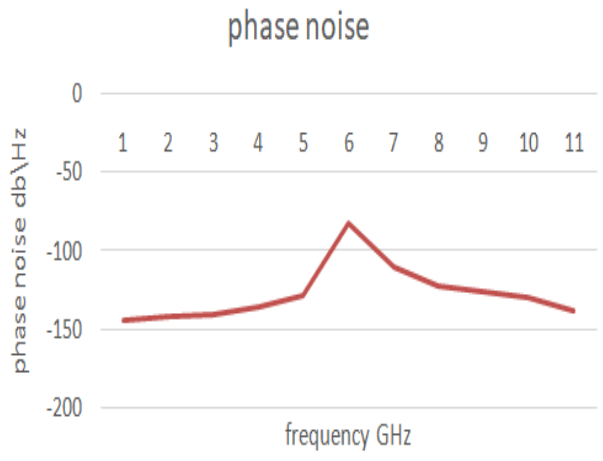

Fig.5*Phase Noise vs frequency plot*

Where L((Δf) is the phase noise form the oscillating frequency fosc, and pdc, pavg is the power ratings of the VCO, T is absolute temperature.

IV. CONCLUSIONS

In this work, a high-performance and low-phase noise VCO with a good figure of merit of -189 dBc/Hz and phase noise of -119 dBc/Hz is achieved. Since a lower technology node is used in designing the VCO with good performance, a lesser chip area is utilized by this VCO when compared to other designs of higher technology nodes. Because of the smaller VCO size radars can be made compact and portable which is the main objective of this work. linearity is an important parameter in designing the oscillator and through this design, good linearity is achieved making the radar vary the transmitting frequencies over a wide range and covering a wide range of distances. Since the cascaded structure is used in this design leakage power is reduced when in a steady state and this cascade structure also helps in reducing the supply variations which reduces the signal to noise ratio. Through this design, lower phase noise can be achieved.

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