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COMPLEMENTARY DUAL MODULAR REDUNDANCY WITH MULTIPLEXER CIRCUIT FOR SOFT-ERROR-TOLERANT DESIGN

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Abstract:

The Dual modular redundancy (DMR) uses two identical modules and a voting circuit, is an existing architecture for soft-error tolerance. To overcome these designs, a complementary dual-modular redundancy (CDMR) with multiplexer scheme is proposed for tolerating many soft errors. It improves the area overhead by tradingoff reliability and vulnerability of the voting system. Based on Markov Random Field (MRF) theory, the voting system is implemented in CDMR and the multiplexer can produce the application of a control signal for a majority value. The CDMR scheme can achieves 12.5% reduction in the error rate and saving the area of one redundant module by reducing 20% of the voting circuit area compared to previous voter designs.

Index Terms— **Markov random field (MRF), soft-error tolerance, Dual modular redundancy (DMR)**

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I. INTRODUCTION

With the advent of VLSI technology have arised the increased complexity and density of VLSI chips, hence high speed digital systems are more liable to defects. The unintended change in design from original design are called Defects. A fault is a representation of a defect reflecting a physical condition that causing a circuit to be failed to perform in a required manner. As the dimension of transistor is increased, the probability of faults occurring in the VLSI systems has also increased.

Fault tolerance means basically ensuring the correct operation instead of fault occurrence, and provides significance of higher reliability. Occurrence of a fault can be internal or external to a function module, but it should not affect the actual output of that function module. If it is ensured, then the fault is said to be masked or successfully hidden from the observer by the outside world. On the contrary, if the fault is not masked, the desired output would be affected from the expected function module by causing an erroneous output to be produced instead of producing the correct output. Hence, faults do not cause an error are said to be masked (concealed) and on the other hand, faults that result in an error are said to be exposed (revealed).

In short, the manifestation of a fault is interpreted as an error. Thus in the electronic systems, occurrence of faults has become common and it is reasonably desirable to incorporate fault tolerant techniques into some designs to ensure reliability. Since adders are the key processing unit of a processor, it becomes necessary to guarantee fault free operation of these units.

Simple faults mainly labelled as the Transient/temporary faults are also called as soft errors because they are correctable. At the logic level, soft errors might tend to get result as single-event effects. Single-event transients (SETs) occur due to high-energy particle strikes, might cause a bit-flip at a gate output node or in interconnects formed between logic elements. An SET possessing sufficient amplitude and duration may be captured by a state-holding element in the system stage and subsequently latched, resulting in an error called as single-event upset (SEU). SEU could also occur when a radiation phenomenon happens to directly the flip, then the binary data output of a register or a memory element which immediately causes an error. SEUs tend to affect data processing by permitting computation with the erroneous data in the successive system stage. However, a transient fault occur as an error depends upon the electrical, logical, and timing masking of the design. Transient faults can be overcome through radiation hardening of underlying combinational and sequential logic and memory elements by employing the redundancy technique.

II. RELATED WORK

The survey focus on about the soft-error in combinational based, voter circuit and logic based circuit,etc. To study about the soft error on the circuits with their results help to analysis the type of error occurred and the techniques needs to tolerance. Soft-error tolerance is an important problem that is needed to be addressed at the circuit, architectural, and algorithmic levels. In all cases, enhancing the robustness of systems and circuits to soft errors introduces redundancy in some form. Doing so results can produce efficient area and power overhead. Therefore, there is a fundamental tradeoff between energy efficiency and robustness. The first survey describes about the types of soft errors and the methods to reduce the errors based on the algorithm and logic. The other survey describes about the error based design and solutions for circuits are defined.

Yufeng, et.al,.[1] Inspired by the Markov Random Field (MRF) theory, a two-stage voting system is proposed in the Complementary Dual Modular Redundancy (CDMR). In MRF based design, the basic elements include feedback loops which help them to achieve high soft-error tolerance. To solve soft error issues in the voter and save area overhead, proposed a new complementary DMR (CDMR) scheme. The MRF design is implemented and produce a NAND-NAND based feedback structure. The stage 2 structure can complement the loss of error tolerance for the first stage using its latch property. For multistage voting design, the voter is added at each stage to improve the overall system reliability. The voter has two outputs without voting duplication with enclosed feedback loops. This produces two complementary outputs as references for error correction.

Lizheng, et.al,.[2] The Autonomous Error Tolerant (AET) architecture aims to have a self-repairing capability and tests the performance variation of AET system under different reliability requirements. The AET structure is designed by the nearby error sensing mechanism to detect the errors

timely, backup circuit switching strategy is used to bypass the failed nodes and active evolution scheme is studied to handle unrecoverable errors. The board-level prototype is used based on dual-core embedded processors. The analysis show that the error tolerant capability is better than the conventional multimodular redundant system.

Robert, et.al,.[3] a dynamic memory core based on Gain-Cell (GC-eDRAM) is used, which is more susceptible to soft errors than a static memory cell. It is a fully logic- compatible implementation which provides a reduced silicon footprint compared with SRAM, but lacks the internal feedback that ensures strong storage levels. Hence, it is used with a circuit-level SEU tolerance by entirely removing the feedback. The transistor count with reduced amount and the physical properties of the dynamic circuit allows to internally apply complementary DMR (CDMR) to achieve per-bit error detection and per-bit error correction.

Ahmad, et.al,.[4] a selective-transistor scaling method is used that protects individual sensitive transistors of a circuit. A sensitive transistor is a transistor whose soft error detection probability is relatively high used until desired circuit reliability is achieved or a given area overhead constraint is met. Transistor duplication and asymmetric transistor sizing are the methods used to applied to protect the most sensitive transistors of the circuit. In asymmetric sizing, nMOS and pMOS transistors are in independent size. Reliability is performed with different protection thresholds and area overhead constraints. Finally, a novel gate level soft error reliability evaluation technique for combinational circuits is proposed that produces similar results as produced by transistor-level simulations.

Amin, et.al,.[5] presents a fast and efficient technique for resizing the large-scale combinational circuits. In this methodology, the circuit is partitioned into a set of smaller subcircuits based on the structures which are originated from the primary outputs (POs). The extracted subcircuits are topologically levelized and then, by starting from the minimum level, the subcircuits located at the same level are resized individually and independently. This procedure is continued level by level until the subcircuits in all levels are resized. During resizing process, after each gate sizing, the subcircuit error probability (SEP) of the subcircuit in which the resized gate is located is computed. Based on the computed SEP, the effects of gate sizing on the total circuit SER are evaluated. Since the SEP computation is much faster than circuit SER computation, evaluating the effects of gate sizing on circuit SER locally by the SEPs results in significantly accelerating in the gate sizing optimization algorithm. This technique is evaluated for various large scale circuits and compared the obtained results with the similar gate sizing optimization approaches.

III. EXISTING METHODOLOGY

In the designs, the basic elements include feedback loops which help them to achieve high soft-error tolerance. However, these implementations require higher area overhead with low reliability. To solve soft-error issues in the voter and save area overhead, proposed a new complementary DMR (CDMR) scheme; The CDMR scheme ensures the signifies of soft-error tolerance even for the voting circuit. This can be achieved by separately processing one module (M1) through a structure with a stable logic “1” as output, and processing another identical module (M2) through a structure with a stable logic “0” as output.

Another feedback structure is then used to merge the stable logic"1" and stable logic "0" outputs from the first stage. The CDMR scheme performs the existing designs in two aspects: 1) tolerating soft errors when propagated to the voting circuit and 2) saving the area overhead.

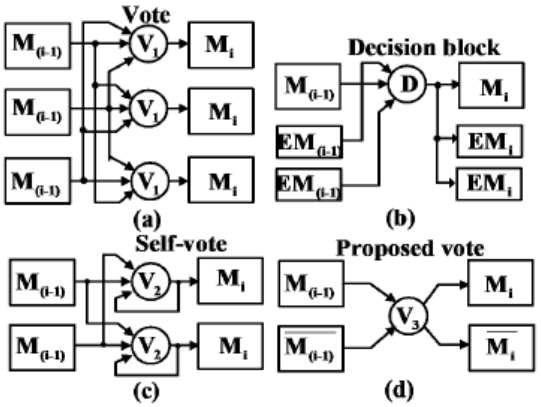

Fig 1: Conventional Voting structure in multistage design (a) TMR (b) FGSET (c) DMR (d) existing voting module

The existing design has achieved soft-error tolerance.. TMR can only tolerate soft errors when the probability of three or two modules failing at the same time is much lower than that of a single module.

For multistage logic, the voter is concatenated at each stage to improve the overall system reliability, as shown in Fig. (a)–(d). The original TMR, FGSET, and DMR voters for multistage are simply duplicated [refer to Fig. (a)–(c)]. However, the proposed voter has two outputs without voting duplication between two stages and computed with the enclosed feedback loops, as shown in Fig. (d). Note that two complementary outputs as references for error correction are obtained. Overall of these designs, area overhead is reduced by at least 50% compared to the designs used in TMR and DMR.

IV. PROPOSED METHODOLOGIES

In this, two-stage CDMR is performed with the multiplexer to increase the ability of the design for saving the area overhead propagating with multiple module system. The MRF inspired voter is implemented in CDMR by substituting an inverting module for one of the identical modules. The MRF based design is based on the energy function specifically the clique energy. The CDMR ensures the soft error tolerance for the voting circuit. In these designs, four modules are referred to a separate structure A, B, C, D which comes under stage 1. The module (M1) and module (M3) are processed with stable logic '0' as outputs and another identical module (M2) and module (M4) are processed with stable logic '1' as outputs. Then next structure is used to merge the stable logic '1' and '0' outputs from the first stage as structure E and F, ensuring the best performance from the first stage.

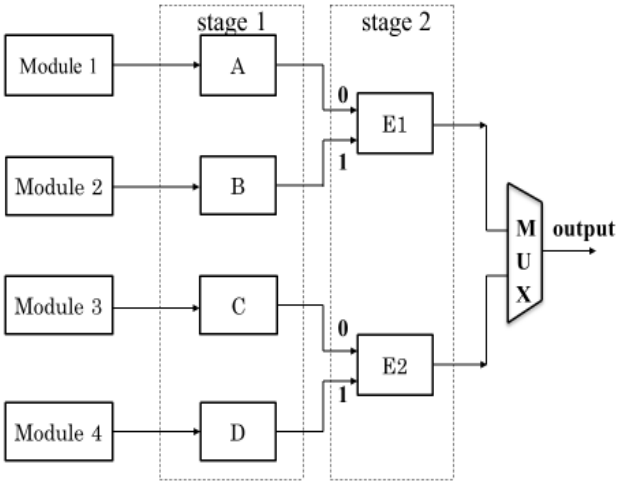

Fig 2: CDMR design with Multiplexer

For the first stage using its latching property, the design can complement the loss of the error tolerance. The structure benefits from the presence

of stage 2 to improve its reliability, which is a feature that CDMR with multiplexer or other designs lack. Let the single-error assumption for stage 1, assuming that only one error can emerge from one of the complementary propagation chains at the same time. In other words, when an error occurs from stage 1, the latch structure of G1-G2 and G3-G4 in stage 2 does not propagate errors received from stage 1. With respect to our proposed CDMR with multiplexer, the two redundant inputs to the voter must be complementary. The multiplexer can produce the controlled high signal based on majority voter.

In the design, the values will propagate through stages 1 and 2 as complementary signals in the absence of errors. For example, an ideal input bit stream for x_a ($x_a = x_b$) in the first branch is {x_0~ $x_4 = 0$ and x_5~ $x_9 = 1$}. Their corresponding bits in the other branch are robust "1" because of the high tolerance of noisy input bit "0" in both AND gates. This consider the cases only where errors occur in weak "0". This condition causes the first stage to remain in the hold state acting as an RS latch, thus protecting the final output results from the influence of the error bits based on the previous correct outputs.

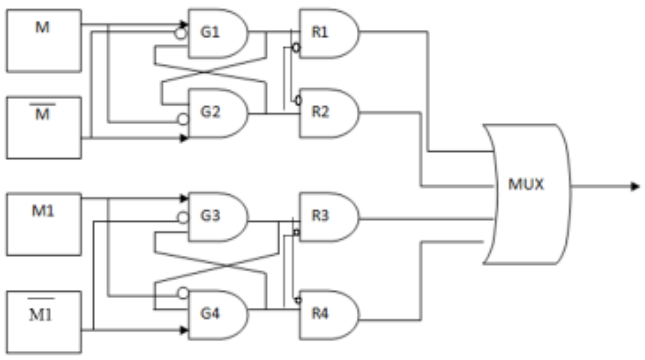

Fig 3: Proposed Structures

Compared with a longer pulse at the output of a TMR voter when an error hits on one of its inner branches, it can be regarded to be less harmless in the proposed structure after sampling, as the error is too short to be sampled multiple times. In the extended one error condition, the output of our module can achieve correct operation as long as the output of the inner complementary signals are not in error at the same time.

4.1 Techniques used in DMR

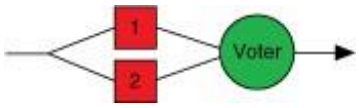

Fig 4: Dual Modular Redundancies

Dual Modular Redundancy (DMR) uses two functional equivalent units, thus it can either control the Digital Up Conversion (DUC). The most challenging aspect of DMR is to determine when the secondary unit is to be switched. Because both units are functioning at the same time, you have to decide what to do if they disagree. You either need to create a tiebreaker vote or a default winner to be the secondary unit, assuming that is more trustworthy than the primary unit. You may be able to trust more the secondary unit normally if the primary is in control and the required functions are run on the secondary to help insure its reliability, but this is very application specific. The multiplexer can be combined to produce the control fixed signal of the trusted unit.

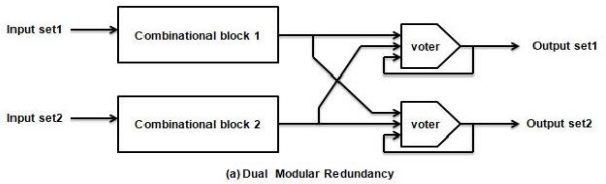

Fig 5: Dual Modular Redundancy Techniques

4.1.1 Time redundancy techniques

Computation Encode Data Decode result Store result Compare results Store result time t0 time t0+d Data error Attempt to reduce the amount of extra hardware at the expense of using additional time

1. Repetition of computations - compare the results to detect faults - re-execute computations (disagreement disappears or remains) good for transient faults no protection against permanent fault problem of guaranteeing the same data when the execution is performed (after a transient fault system data can be completely corrupted)
2. Use a minimum of extra hardware to detect also permanent faults - encode data before executing the second computation.

4.1.2 Software redundancy techniques

1. Due to the large cost of developing software, most of the software dependability effort has focused on fault prevention techniques and testing strategies
2. Fault tolerant software
3. Multi-version approaches
4. Mainly used in safety-critical systems (due to cost)
5. Single-version approaches one code with error detection and fault tolerant capabilities inside

V. EXPERIMENTAL RESULTS

To demonstrate the inherent ability of the error tolerance in the voting circuit, the output shows consistent results at the final stage and the desired outcome is obtained. As shown in the Fig. there is a propagation of a signal injected by a soft error is kept to be hold and then recomputing a error bit, it produces the correct output. By this, it is used to redundant the errors while it is propagating to the internal or external of the system.

Experimental conditions include the simulation tool of Xilinx and the result is viewed in Modelsim, Any Intel x64 Processor, CPU 2.2 GHz min, RAM Memory 2048 MB and 64-bit Microsoft Windows Operating System. In this project, the proposed scheme is implemented with 8 x 8 router handling the error tolerant design. The input bits are applied to the modules with the proposed redundancy technique. It improves the performance of the system by enabling the inputs to a desired output. In addition, these techniques have less impact on timing performance.

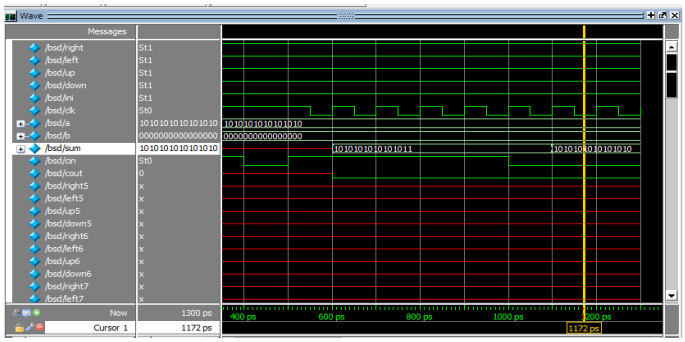

Fig 6: Simulation result of soft-error tolerance

Explanation: The input level of 1s and 0s bits are used. When the input is increased to be changed, the output will also be changed. If any input vote to be missed in the circuit, then the error occurs.When the input level is increased then the bits are added and it produces the correct output which reduces the errors in the redundancy circuit.

VI. CONCLUSION

The Complementary Dual modular redundancy (CDMR) with multiplexer modules and a voting circuit, is proposed for soft-error tolerance. In the proposed CDMR, multiplexers could be added to increase the ability of the design and it

also improves the reliability of the design. The design was implemented by Xilinx and Modelsim to achieve better soft-error tolerance. In the future work of the project, compared to MRF – inspired voting system some other techniques could be used to increase the testability of the design and improve the error tolerance with the multiple voter.

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