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Design of 256 channel Re-configurable Sample Rate Converter for Accelerated 3T-MRI

Dr. Navneet Agrawal*, Himangi Agrawal**, Gaurav Vasita***, Dr. Suriti Gupta****

*(Professor & Head, Department of Electronics and Communication Engineering, CTAE, MPUAT, Udaipur, India
Email: navneetctae@gmail.com)

** (Associate Engineer (ASIC Division), E-Infochips Pvt. Ltd., Ahmedabad, Gujarat, India
Email: himangi2807@gmail.com)

*** (SRF, Department of Electronics and Communication Engineering, CTAE, MPUAT, Udaipur, India
Email: gauravvasita99@gmail.com)

**** (Asstt. Professor, Department of Electronics and Communication Engineering, CTAE, MPUAT, Udaipur, India
Email: suriti82@yahoo.co.in)

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Abstract:

Current paper presents a low-latency, scalable and FPGA-implementable 256-channel re-configurable sample rate converter optimized for high-throughput medical systems like 3T-MRI machines. The architecture eliminates the need for filters or DSPs (Digital Signal Processing)by using per-channel buffering, counter-based decimation, and indexed output sequencing, resulting in a design that is resource-efficient, real-time, and deployable on FPGAs (Field Programmable Gate Arrays) with limited I/O (Input-outputs). The design supports 100 MHz operation and is validated through simulation and synthesis, offering significant improvements over traditional converter architectures.

Keywords — **DSPs (Digital Signal Processing), FPGAs (Field Programmable Gate Arrays), MRI (Magnetic Resonance Imaging), ADC(Analog to Digital Converter)**

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I. INTRODUCTION

Current study is designed to be suitable for clinical and research imaging, especially in cardiology and advanced neurology applications. A medical professional can identify subtle details deep within the body due to the higher signal-to-noise ratio, while taking a fraction of the time to scan the patient. The proposed system would be developed by Reconfigurable 256-channels sample rate convertor which is to be used for base band echo signals to regulate the sample rate in medical imaging applications in Magnetic resonance imaging (MRI)[2]. This development can open new doors in cardiac, brain and abdominal MRI with the increase in speed of diagnosis and sensitivity. The potential applications of 256-channel MRI scanning would increase the image resolution and parallel imaging with larger speed. It would be capable to down sample the prevailing highly oversampled echo signal by an integer factor at run time.

We wish to investigate and develop 256 channels 3T-MRI system to deliver better imaging and improve the speed of acquisition giving more than 20-fold acceleration with very low g-factor (noise-amplification factor). This will not only help critical patients but open the doors in medical science to diagnose or early detection of the disease saving thousands of lives. These anticipated results have motivated us to design a 256-channel fractional sample rate convertor for accelerated in-vivo 3T-MRI[4].

MRI machines, particularly 3T-MRI systems, utilize an array of coil elements to capture detailed anatomical images. These coils generate analog signals that are digitized and processed simultaneously with the help of A-to-D converters (ADC). The output of these ADCs is often sampled at high rates and must be down sampled (decimated)

before further processing or storage. Traditional sample rate conversion architectures used in MRI systems include:

- CIC (Cascaded Integrator-Comb) Filters
- Polyphase Filters

While effective in general DSP applications, these approaches suffer from key drawbacks when applied to large-scale channel environments like 3T-MRI:

- High Latency: Due to multiple filtering stages and feedback loops.
- Heavy DSP Block Usage: Requires numerous multipliers and accumulators.
- Scalability Issues: Complexity and resource consumption grow exponentially with channel count.
- Implementation Barriers: These designs are not optimized for FPGA platforms with constrained I/O and logic resources.

There exists a need for a low-latency, filter-free, scalable, and FPGA-implementable sample rate converter that can handle 256 parallel input channels, with timing and power efficiency.

The current paper relates to the domain of digital signal processing (DSP) and hardware design for medical imaging equipment. More specifically, it pertains to the development and implementation of a 256-channel sample rate converter, optimized for 3 Tesla Magnetic Resonance Imaging (3T-MRI) systems[2]. This design enables simultaneous, real-time, and resource-efficient down sampling of high-throughput parallel data streams acquired from multiple MRI receiver channels, facilitating efficient data handling for further processing and reconstruction.

II. LITERATURE REVIEW

International status: In 2006 Massachusetts General Hospital (MGH) and Siemens Medical Solutions developed in partnership a prototype 128-channel magnetic resonance imaging (MRI) system that is built from Siemens' MAGNETOM Trio with Tim 3 Tesla (3T) MRI system. Specifically, the prototype is based on the 102X32 Tim architecture (with 102 coil elements integrated in 32 independent radio frequency (RF) channels) that has been expanded to 128 independent RF channels and coil elements.

The potential applications of 128-channel MRI scanning are being evaluated at MGH. Findings thus far have shown the potential to exceed current standards of image resolution and parallel imaging, with up to 25 times the speed[1].

National status: In India most of the hospitals provide the facility of MRI. Most of the established hospitals and their chain of canters throughout India are making use of either 32 channels or very rare 128 channel MRI systems. We have reviewed the status of following hospitals and identified their limitations for MRI imaging:

- Apollo Hospital Group , India
- Artemis Hospital, Gurgaon (Delhi)
- BGS Global Hospitals Group, India
- Escorts Heart Institute Hospital, Delhi
- Fortis Hospitals Group, India
- Manipal Hospital, Bangalore
- Max Hospitals Group, India
- MIOT Hospital, Chennai
- Narayana Hospitals Health city, Bangalore
- Sparsh Hospital, Bangalore
- Wockhardt Hospitals Group, India

Based on above literature review and live survey, we have designed our problem statement and carried out the study to get possible solution for reconfigurable sample rate converter for 3T-MRI.

III. WORK PLAN AND METHODOLOGY

For the proposed research work we acquired the skill using the following tools for simulation.

A. *Xilinx ISE*

Xilinx Integrated Software Environment (ISE). ISE tool provide the facility of simulate and implement of any combinational & sequential circuit. It generates the synthesized report of digital circuits for any family of FPGA board. Hardware description language is used to develop design of 256 channel sample rate converter for

3TMRI Machine on Xilinx ISE. In current research work the used version of Xilinx ISE is 14.4

B. ***Xilinx Plan Ahead***

By using Plan Ahead tool better circuit performance is obtained by using different ways of implementation, improve timing constraints, and apply physical constraints with floor planning techniques. Plan ahead also provides the facility to measure resource utilization, interconnect delay, power consumption[8]. Routing connectivity assists with appropriate logic design, device selection and floor planning. In current research work the used version of Xilinx Plan Ahead is 14.4.

C. Generation of Verilog coder for Implemented design

With the help of system generator tool box of Xilinx Block set we generate the Verilog code for our design in our current research work.

D. Estimation of Resources utilization on FPGA using Xilinx ISE Design Suit

The Estimation of Resources utilization of multichannel sample rate convertor is done on FPGA after executing the following steps:

- Checking the syntax for the code by simulation.
- Synthesis report for resource utilization table.

The complete integrated 256-channel reconfigurable sample rate converter design is carried out with the help of following sequential steps.

Step 1: Development of CIC (Cascaded Integrator Comb) decimator

Step 2: Development of 2 channel sample rate converter and development of 8 channel sample rate converter using 4:1 multiplexer.

Step 3: Extension of 8 channel sample rate converter into 256-channel sample rate converter using 2: 1 multiplexer.

Step 4: Development of 8 bit counter to control select pins of 256:1 MUX.

Step 5: Development of FIFO with depth 256 and width 8 with full and empty flags.

Step 6: Development of FSM to control full and empty flags.

Step 7: Assembling of all the above steps with proper interfaces to finally design RTL of 256 channel sample rate converter

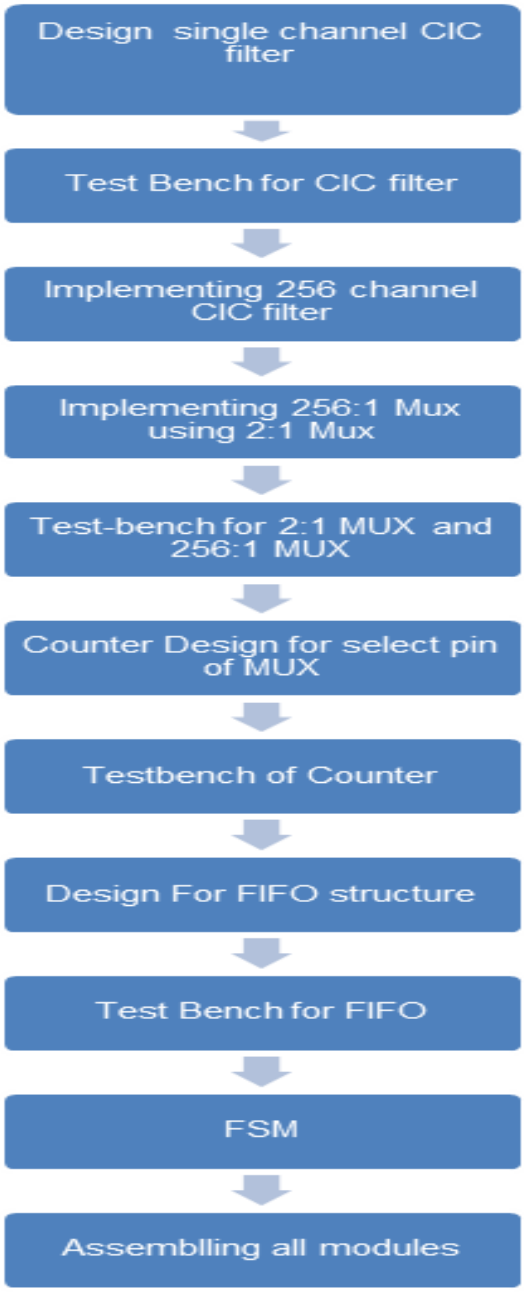

Fig 1. Flow Chart to Implement Sample Rate Convertor

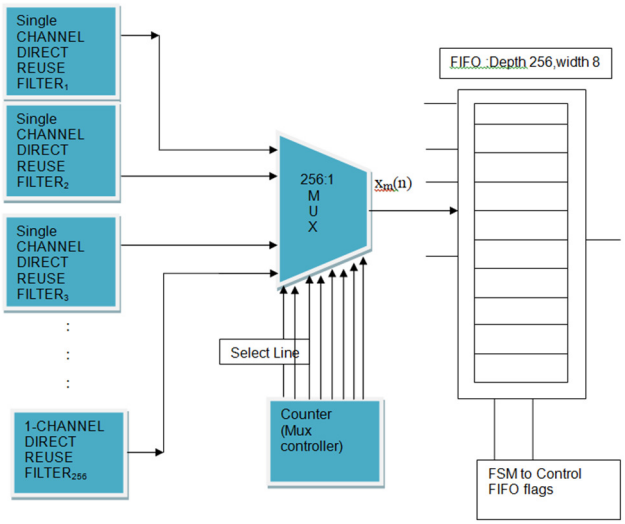

Fig 2. 256-channel sample rate convertor block diagram

IV. RESULTS AND DISCUSSION

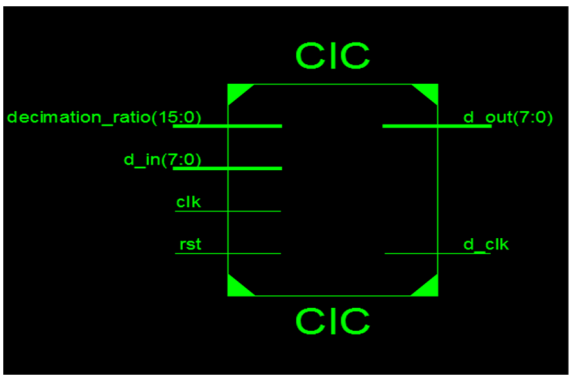

Fig 3. CIC Decimator

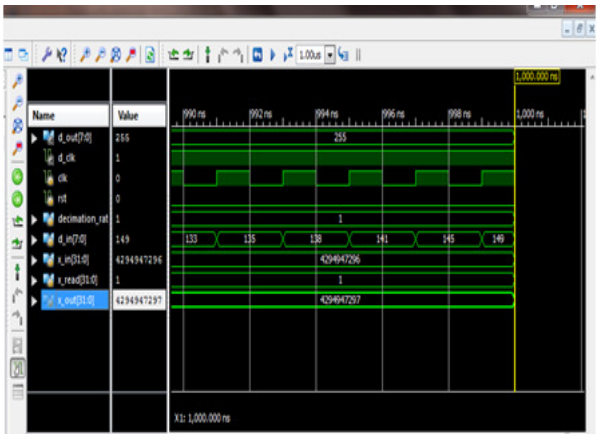

Fig 4. CIC Decimator Waveforms

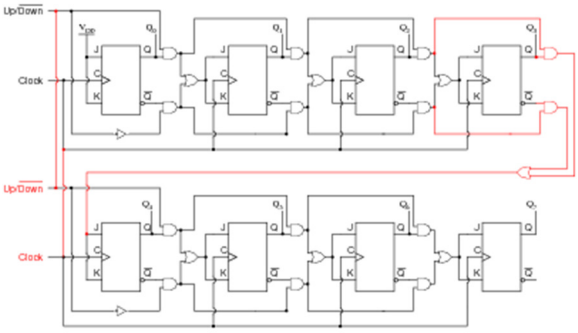

Fig.5. 8 Bits Counter Design

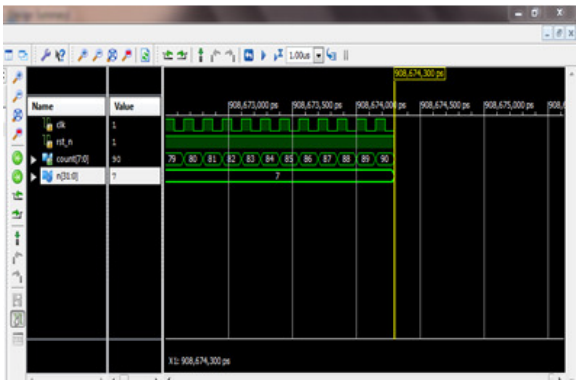

Fig.6. 8 Bits Counter output

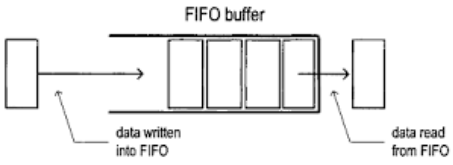

Fig 7. FIFO buffer

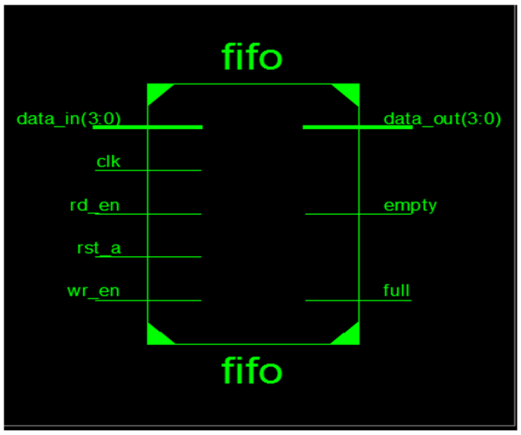

Fig 8. FIFO Read and Write Module

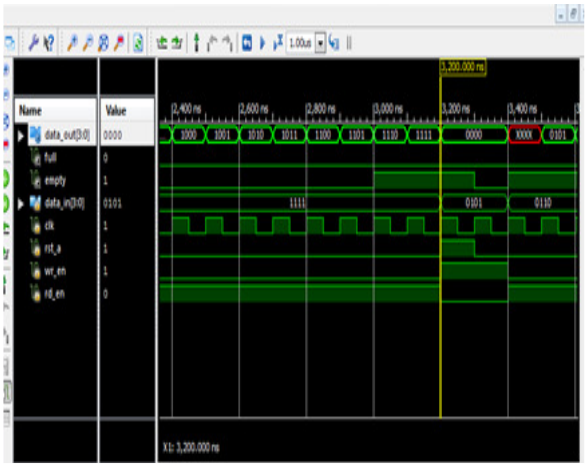

Fig 9. Write data Into FIFO Module

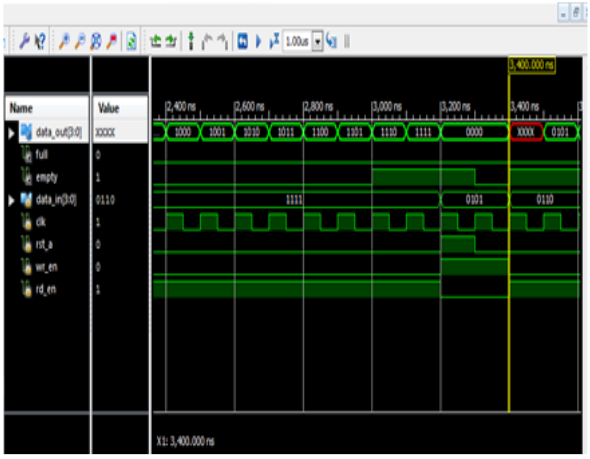

Fig 10. Read data from FIFO Module

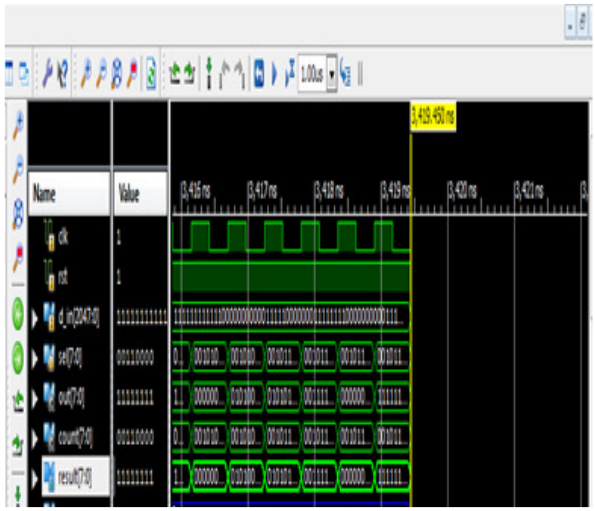

Fig.11 256:1 Multiplexer Result

V. CONCLUSIONS

From the above results it is concluded that there is a need to increase resolution and speed with less delay. It is also observed that there will not be much effect of power consumption as already the device is working on high power consumption, thus design may or may not be low power but the most important criterion for designing of sample rate converter will be its high speed and reduced delay. High field strength increases the pitch of noise so the issue of noise also remains a point of further research which is to be addressed in future research whenever one wish to carryout study from 3t MRI to 7T MRI. The research outcome will benefit not only to the residents of Rajasthan but it will cater advanced medical facility to human kind. Critical details of the human body tissues, which cannot be diagnosed by the available MRI machines due to limited sample rate, will be easily handled by the doctors after successful implementation of this project. This may help clinically to whole of the society at large creating advance facilities in India itself at par with medical facilities available abroad.

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