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# Comparative Analysis of Modulation Techniques for Five-level Inverters in Grid-Tied Photovoltaic Applications

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## Abstract
The efficiency of power conversion systems is critical to the global transition toward decentralised renewable energy grids. This paper presents a comparative analysis of three modulation strategies applied to a three-phase, five-level Neutral Point Clamped (NPC) inverter in a grid-tied photovoltaic (PV) context: Phase Disposition Sinusoidal Pulse Width Modulation (PD-SPWM), Space Vector Pulse Width Modulation (SVPWM), and Selective Harmonic Elimination (SHE). All techniques are implemented in MATLAB/Simulink environment and evaluated against IEEE 1547 and IEC 61727 standards using Total Harmonic Distortion (THD), DC-bus utilisation (Voltage Utilisation Factor, VUF), and Common-Mode Voltage (CMV) suppression as primary metrics. A key finding is that, under the LCL filter optimised for the carrier-based methods, five-level SVPWM does not meet the IEEE 1547 THD limit, yielding an 8.43% filtered THD; a sensitivity analysis (Section IV.F) shows this non-compliance is filter-bound rather than intrinsic to the modulation strategy. PD-SPWM achieves the lowest filtered THD of 1.01% and the highest VUF of 49.75%, while SHE achieves 2.69% THD, the lowest peak CMV of ±72 V, and the lowest switching frequency of 450 Hz, making it thermally optimal. This trivariate comparison, THD, CMV, and VUF measured simultaneously across all three strategies under an identical five-level NPC topology, consolidates within a single model metrics that prior work has examined only separately or in pairs. SHE is recommended as the thermally optimal strategy for utility-scale PV systems; PD-SPWM is recommended where power quality is the primary constraint.

*Index Terms—Common-mode voltage, five-level inverter, modulation techniques, neutral point clamped inverter, photovoltaic systems, selective harmonic elimination, space vector PWM, total harmonic distortion.*

## I. Introduction

Global energy infrastructure is undergoing a rapid transition from centralised fossil-fuel generation to decentralised renewable resources. Grid-connected photovoltaic (PV) systems have evolved from a supplemental role into a core component of modern energy infrastructure [1]. Solar panels produce direct current (DC), which inverters must convert to alternating current (AC) for grid integration.

Traditional two-level inverters have served as the industry benchmark due to their simplicity and relatively lower cost [2]. However, they impose high switch stress; each device must block the full DC-link voltage and generate significant harmonic distortion, requiring large, costly filters [3]. These limitations motivate the adoption of Multilevel Inverters (MLIs), which produce a 'staircase' waveform that closely approximates a sinusoid before filtering, reducing electromagnetic interference (EMI) and filter size requirements [4].

Among MLI topologies, the five-level Neutral Point Clamped (NPC) inverter has gained prominence in grid-tied PV systems [2]. Three principal modulation strategies are applied to such inverters: PD-SPWM, SVPWM, and SHE. These techniques present conflicting trade-offs between harmonic quality, DC-bus utilisation, and CMV suppression. Although each strategy has been studied individually, few studies report THD, CMV, and VUF simultaneously across all three strategies under an identical five-level NPC topology and LCL filter [5]. The widely cited 15.5% DC-bus utilisation advantage of SVPWM over SPWM is derived exclusively for two-level inverters and routinely extrapolated to five-level systems without empirical validation [6]. This paper fills that gap.

The specific contributions of this work are:

1) A validated MATLAB/Simulink model of a three-phase five-level NPC inverter with P&O MPPT and LCL filter interface, parameterised for a 415 V, 50 Hz grid.

2) Implementation of PD-SPWM, SVPWM with g-h coordinate transformation, and SHE with GA-based offline angle optimisation and LUT integration.

3) The first simultaneous trivariate comparison of THD, CMV, and VUF for all three strategies under identical five-level NPC conditions.

4) Empirical evidence that, under an LCL filter tuned for the carrier-based methods, five-level SVPWM yields 8.43% filtered THD and is non-compliant with IEEE 1547 in this configuration; Section IV.F shows the non-compliance is filter-bound rather than intrinsic to the modulation strategy.

5) A dynamic irradiance stress test showing SVPWM THD degrades to 11.20% at low irradiance under the carrier-tuned filter, indicating an operating-point sensitivity to be addressed through filter co-design.

## II. Background and Related Work

### *A. Five-Level NPC Topology*

The NPC inverter, introduced by Nabae et al. [1], achieves multiple voltage levels through series-connected DC-link capacitors and clamping diodes. In the five-level configuration, four capacitors divide the DC bus into five output levels ($\pm 2V^{Dc}$, $\pm V^{Dc}$, 0), reducing switch voltage stress to $V^{Dc}/4$ and enabling finer waveform synthesis before

  

filtering [7]. Fig. 1 illustrates the characteristic five-level phase voltage and the resulting nine-level line-to-line voltage ($V_{ab} = V_{an} - V_{bn}$) that further reduces harmonic content.

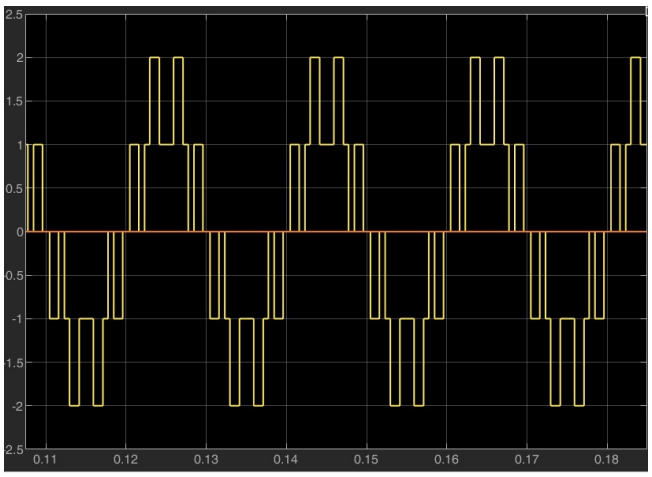


**Fig. 1.** Five-level phase voltage gate pulse transitions, showing the staircase from $\pm 2V^{Dc}$ to $\pm V^{Dc}$ and 0.

IEEE 1547-2018 mandates THD below 5% and specifies voltage regulation and reactive power requirements. IEC 61727 defines current distortion and flicker limits. IEC 62109 addresses leakage current suppression in transformerless configurations, directly linking CMV characteristics to compliance [9].

### *B. PD-SPWM*

Phase Disposition SPWM uses (m−1) in-phase triangular carriers compared against a sinusoidal reference. For a five-level inverter, four carriers are stacked across the DC bus. PD-SPWM concentrates distortion in high-frequency sidebands near $2f^c$ that the LCL filter attenuates efficiently [10]. However, its high switching frequency (typically 5 kHz) increases IGBT thermal stress [11].

### *C. SVPWM*

Space Vector PWM treats the three-phase inverter as a single entity on an (α, β) plane. A five-level NPC produces $5^3 = 125$ switching states forming a hexagonal diagram with six major sectors and 61 triangular sub-sectors [12]. The 15.5% DC-bus utilisation gain over SPWM cited in the literature is demonstrated only for two-level and three-level inverters [6]. At five levels, the 61-sector logic introduces switching jitter and pulse-width quantisation errors not previously quantified against PD-SPWM or SHE [13]. The g-h coordinate transformation (60° non-orthogonal frame) replaces trigonometric sector identification with integer floor operations, reducing computational load [14].

### *D. Selective Harmonic Elimination*

SHE pre-computes switching angles by solving non-linear transcendental equations derived from Fourier analysis of the staircase output. For a five-level NPC with N = 5 switching angles per quarter-cycle, the fundamental is controlled, and the 5th, 7th, 11th, and 13th harmonics are eliminated analytically [15]. The Newton-Raphson (N-R) method solves these equations iteratively but exhibits Jacobian singularity at extreme modulation indices [16]. GA optimisation overcomes this limitation as a stochastic global search, yielding valid angle sets across the full modulation-index range [17]. SHE operates at ~450 Hz, significantly reducing switching losses, but requires a pre-computed LUT for real-time operation [18].

### *E. Research Gap*

The literature reveals three specific gaps. First, although DC-link balancing, CMV, and THD are treated jointly for NPC inverters in review studies, no reviewed work reports all three metrics simultaneously for PD-SPWM, SVPWM, and SHE under an identical five-level NPC topology [5], [19]. Second, the SVPWM DC-bus utilisation advantage is extrapolated from two-level literature without five-level empirical validation [6], [20]. Third, SVPWM harmonic performance at five levels has not been compared to PD-SPWM or SHE in any reviewed paper [12], [13].

## III. METHODOLOGY

### *A. Topology and Simulation Environment*

The simulation platform is a three-phase, five-level NPC inverter modelled in MATLAB/Simulink with the Simscape Electrical toolbox. Each phase leg contains eight IGBTs; four series-connected 2200 µF DC-link capacitors divide the 800 V bus into segments of $V^{Dc}/4 = 200$ V per device. Clamping diodes constrain each switch to block no more than $V^{Dc}/4$, reducing dV/dt stress and EMI. The PV source is modelled with dynamic irradiance (0.25 Hz sinusoid, 200–1000 W/m²) and a P&O MPPT boost converter maintaining 800 V DC-link. A fixed-step solver (ode4 Runge-Kutta, $T_s = 5$ µs) satisfies the Nyquist criterion for the 50th harmonic (2500 Hz) per IEC 61000-4-7. Key simulation parameters are given in Table I.

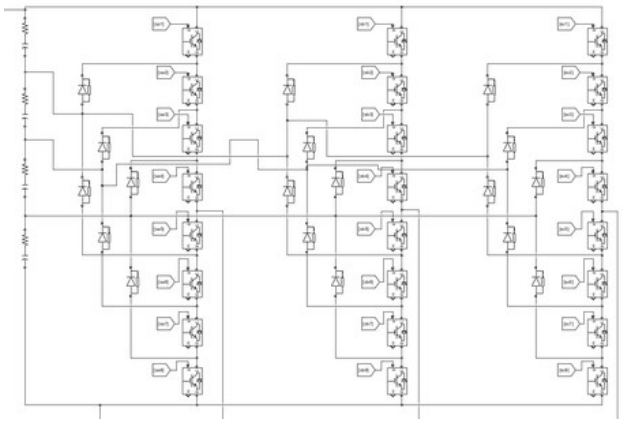

**Fig. 2.** Physical architecture of the five-level NPC inverter.

  

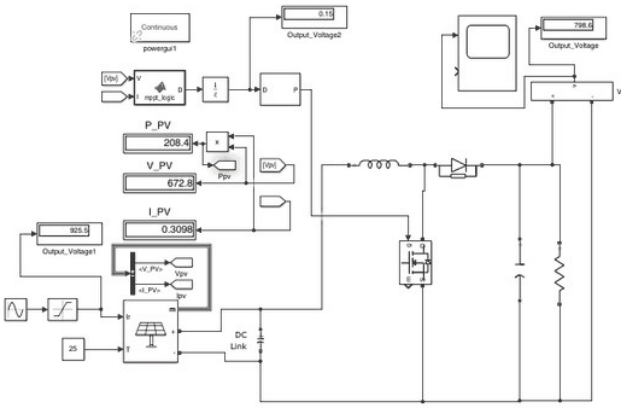


**Fig. 3.** PV array and MPPT implementation.

TABLE I

Simulation Parameters

| Parameter | Symbol | Value |
|---|---|---|
| Fundamental Frequency | f | 50 Hz |
| Carrier Frequency (PD-SPWM) | $f^c$ | 5000 Hz |
| DC Bus Voltage | $V^{Dc}$ | 800 V |
| Inverter-Side Inductance | $L_i$ | 150 mH |
| Grid-Side Inductance | $L^g$ | 10 mH |
| Filter Capacitance | $C^f$ | 15 µF |
| Modulation Index | $m_a$ | 0.85 |

### *B. LCL Filter Design*

An LCL filter ($L_i = 150$ mH, $C^f = 15$ µF, $L^g = 10$ mH) interfaces the inverter to the 415 V, 50 Hz grid. The resonant frequency $f\_res \approx 503$ Hz satisfies the IEEE 1547-2018 stability criterion $10 \cdot f\_grid < f\_res < 0.5 \cdot f\_sw$ (500 Hz < 503 Hz < 2500 Hz). A passive damping resistor $R^D$ in parallel with $C^f$ prevents resonance amplification.

### *C. PD-SPWM Implementation*

Four in-phase triangular carriers ($C_1$ to $C_4$) are stacked across the DC bus range and compared against a 50 Hz sinusoidal reference V_ref for each phase ($m_a = 1.0$, $m^f = 100$). The five output levels are selected by comparator-OR logic per phase. In-phase carrier symmetry causes carrier-frequency harmonics to be common-mode; line-to-line subtraction cancels them, shifting residual energy to ~$2f^c$ (10 kHz) where LCL attenuation is maximum.

### *D. SVPWM with g-h Transformation*

The g-h coordinate transformation shifts the vector representation from the orthogonal α–β frame to a 60° non-orthogonal plane:

$$g = (3/2)V\alpha + (1/2)V\beta, \quad h = V\beta \quad (1)$$

Sub-sector boundaries align with integer coordinates in the g-h frame, enabling floor-function identification without trigonometric computation. Dwell times $d_1$, $d_2$, and $d_3$ are computed as linear expressions of fractional remainders. Redundant switching states balance the four DC-link capacitors in real time.

### *E. SHE Implementation*

Five switching angles ($\alpha_1$–$\alpha_5$) per quarter-cycle control the fundamental and eliminate the 5th, 7th, 11th, and 13th harmonics:

$$(4V^{Dc}/\pi)\,\Sigma\cos(\alpha_i) = M \quad (2)$$

$$\Sigma\cos(n\alpha_i) = 0, \quad n \in \{5, 7, 11, 13\} \quad (3)$$

N-R with a continuation strategy (step $\Delta M = 0.01$) was first applied but failed at $M < 0.4$ and $M > 0.95$ due to Jacobian singularity. A GA solver (population = 60, generations = 400, linear inequality constraints on angle ordering) resolved all operating points, producing a complete 40-point LUT from $M = 0.1$ to $M = 1.15$. During operation, the MPPT block derives M from measured irradiance, and the LUT returns the pre-computed angles via bilinear interpolation.

## IV. Results and Discussion

### *A. Harmonic Performance and IEEE 1547 Compliance*

Table II summarises the THD outcomes. Fig. 5 and Fig. 6 show the PD-SPWM output before and after LCL filtering. The unfiltered spectrum (33.08% THD) is dominated by sidebands concentrated near the 5 kHz carrier frequency. After filtering, the LCL filter's high inductive reactance (~4712 Ω at 5 kHz) attenuates these sidebands to yield 1.01% filtered THD well within the IEEE 1547 5% limit.

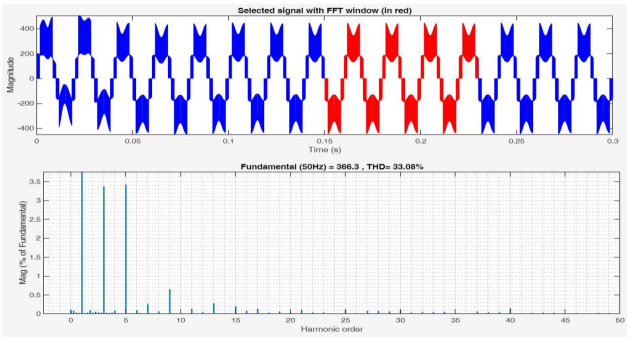


**Fig. 5.** PD-SPWM output before filtering. Harmonic energy is concentrated in high-frequency sidebands around the 5 kHz carrier (unfiltered THD = 33.08%).

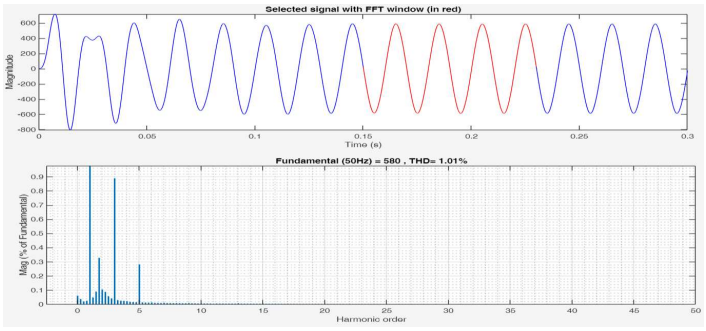


**Fig. 6.** PD-SPWM output after LCL filtering. The clean 50 Hz sinusoid confirms effective sideband attenuation (filtered THD = 1.01%).

  

TABLE II

THD Outcomes and IEEE 1547 Compliance

| Technique | Unfiltered THD (%) | Filtered THD (%) | IEEE 1547 |
|---|---|---|---|
| PD-SPWM | 33.08 | 1.01 | Pass (Superior) |
| SVPWM | 59.84 | 8.43 | Fail |
| SHE | 53.45 | 2.69 | Pass (Optimal) |

Fig. 7 and Fig. 8 present the SVPWM output before and after filtering. The unfiltered spectrum (59.84% THD) shows prominent low-order harmonic content, a qualitatively different pattern from PD-SPWM. The 61-sector logic requires continuous switching between redundant states to balance the DC-link capacitors, producing switching jitter that spreads distortion across the 500 Hz–2000 Hz band. At M = 0.85, narrow dwell times in the outer sub-hexagons are rounded to zero at the 5 µs simulation step, causing pulse-width quantisation errors that inject low-order harmonics. The 150 mH LCL filter presents only ~471 Ω at 500 Hz, insufficient to suppress this broadband low-frequency content, leaving 8.43% residual THD post-filter and failing IEEE 1547.

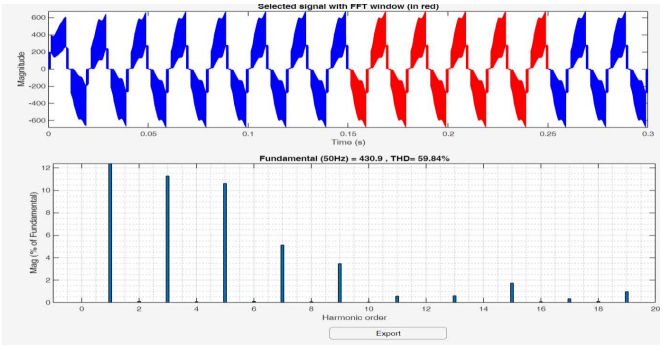


**Fig. 7.** SVPWM output before filtering. Low-order harmonic content from switching jitter and 61-sector quantisation errors dominates the spectrum (unfiltered THD = 59.84%).

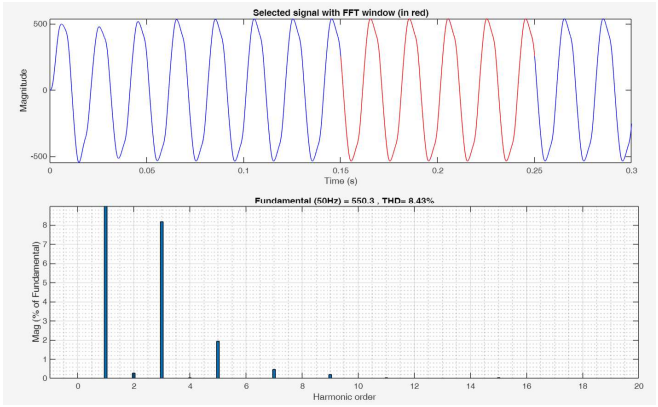


**Fig. 8.** SVPWM output after LCL filtering. Low-order harmonics survive filtration because the 150 mH LCL filter cannot attenuate the 500 Hz–2 kHz distortion band (filtered THD = 8.43%, non-compliant).

Fig. 9 and Fig. 10 show the SHE output before and after filtering. The unfiltered spectrum (53.45% THD) confirms that the 5th, 7th, 11th, and 13th harmonics are near-zero—validating the GA-solved angle sets. The residual content consists predominantly of higher-order harmonics that the LCL filter's inductive reactance suppresses effectively, yielding 2.69% filtered THD within IEEE 1547 compliance.

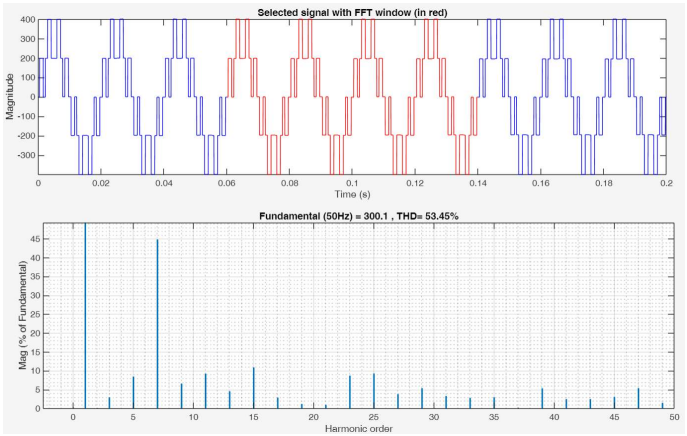


**Fig. 9.** SHE output before filtering. The 5th, 7th, 11th, and 13th harmonics are analytically nulled by the GA-solved switching angles (unfiltered THD = 53.45%).

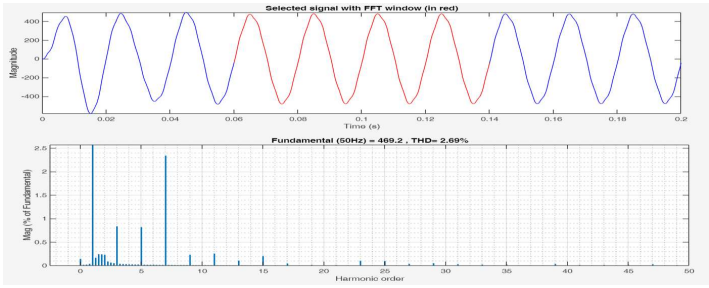


**Fig. 10.** SHE output after LCL filtering. Higher-order harmonics are attenuated effectively, yielding 2.69% filtered THD within IEEE 1547 limits.

### *B. DC-Bus Utilisation*

Table III presents the Voltage Utilisation Factor (VUF = V_out/V_DC) for each technique. Fig. 11 shows the PD-SPWM DC-bus characteristics: the output fundamental (blue) stabilises at 398 V from an 800 V bus (VUF = 49.75%), enabling the inverter to match grid voltage requirements without excessive PV array boosting.

  

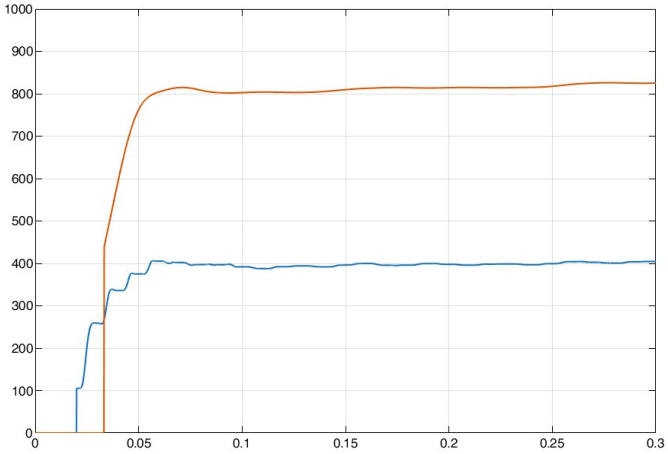


**Fig. 11.** DC utilisation for PD-SPWM. DC-link voltage (orange) settles at 800 V; output fundamental (blue) reaches 398 V (VUF = 49.75%).

TABLE III

DC-Link Utilisation and Voltage Utilisation Factor

| Technique | $V^{Dc}$ (V) | V_out (V) | VUF (%) |
|---|---|---|---|
| PD-SPWM | 800 | 398 | 49.75 |
| SHE | 801 | 298 | 37.20 |
| SVPWM | 836 | 240 | 28.71 |

Fig. 12 reveals SVPWM's most unexpected result: only 240 V fundamental from a DC-link that rose to 836 V (VUF = 28.71%). This inverts the predicted 15.5% SVPWM advantage over SPWM. The elevated DC-link voltage indicates that the P&O MPPT boost converter compensated for the inverter's poor fundamental extraction. The VUF deficit is consistent with an implementation-related cause—reference scaling, over-modulation handling, or the dwell-time quantisation noted in Section IV.A—rather than an intrinsic property of SVPWM; isolating the dominant factor is identified as future work. Fig. 13 shows the SHE DC characteristics: a VUF of 37.20% (298 V from 801 V), reflecting the mathematically expected fundamental reduction when switching angles are constrained to null specific harmonic orders.

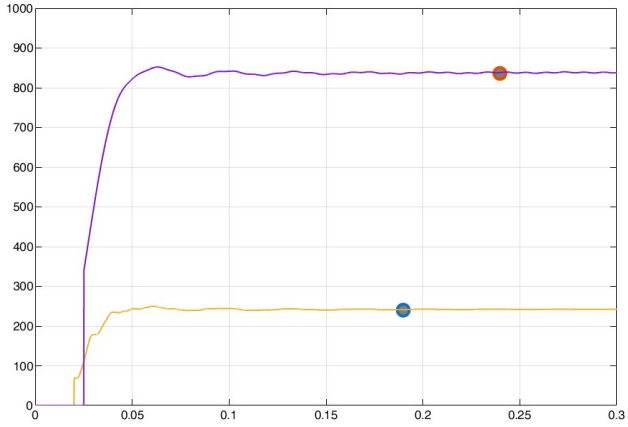


**Fig. 12.** DC utilisation for SVPWM. DC-link (purple) rises to 836 V while output fundamental (orange) reaches only 240 V (VUF = 28.71%), inverting the predicted SVPWM advantage.

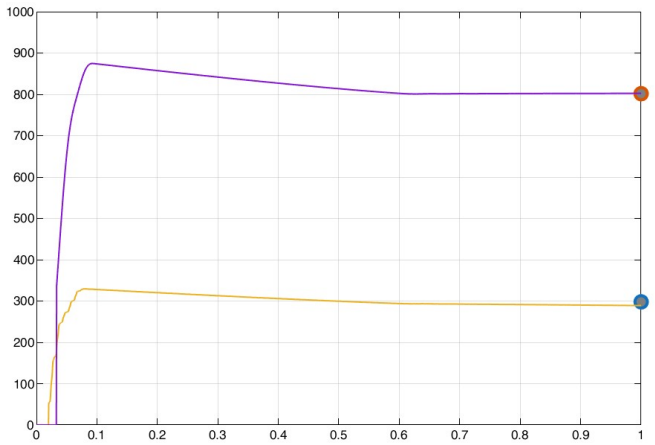


**Fig. 13.** DC utilisation for SHE. DC-link (purple) settles at 801 V; output fundamental (orange) reaches 298 V (VUF = 37.20%).

### *C. Common-Mode Voltage Analysis*

Table IV summarises CMV performance. Fig. 14 shows the PD-SPWM CMV waveform: a third-harmonic envelope (±225 V peak, 150 Hz) overlaid with 5 kHz high-frequency ripple. The sustained high dV/dt imposes leakage current stress on PV module insulation and grid transformer windings.

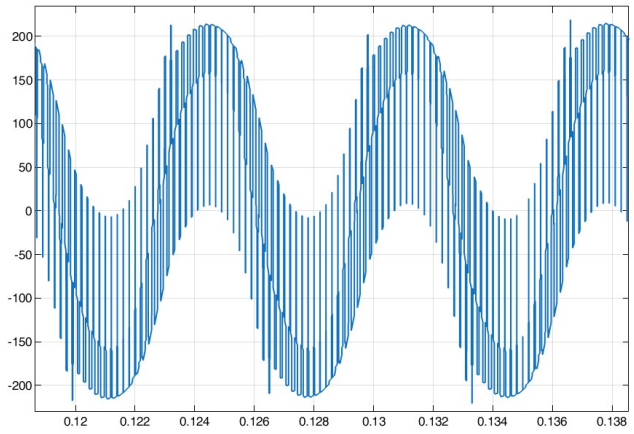


**Fig. 14.** CMV waveform for PD-SPWM. A sinusoidal third-harmonic envelope at 150 Hz with ±225 V peak is modulated by 5 kHz switching ripple.

Fig. 15 shows the SVPWM CMV waveform, which exhibits irregular bursts exceeding ±300 V. These aggressive spikes arise from the continuous redundant-state switching required to balance the DC-link capacitors under the 61-sector algorithm and could exceed safe limits for standard PV panel encapsulant, potentially violating IEC 62109 leakage current thresholds in transformerless configurations.

  

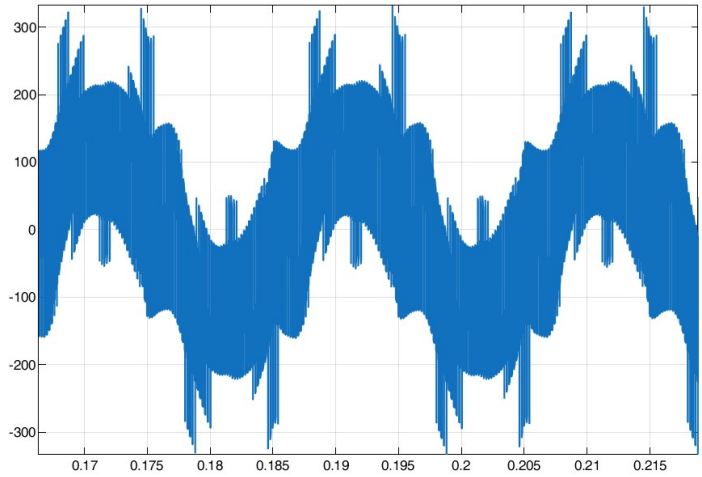


**Fig. 15.** CMV waveform for SVPWM. Irregular bursts exceeding ±300 V result from the continuous redundant-state switching required for neutral-point balancing.

Fig. 16 shows the SHE CMV waveform: periodic, low-density square pulses bounded at ±72 V, a reduction of 68% relative to PD-SPWM and more than 75% relative to SVPWM. The deterministic, infrequent switching transitions create consistent, well-bounded CMV at 450 Hz, minimising high-frequency leakage current paths through parasitic PV-panel capacitances and making SHE the most hardware-friendly strategy for transformerless PV applications.

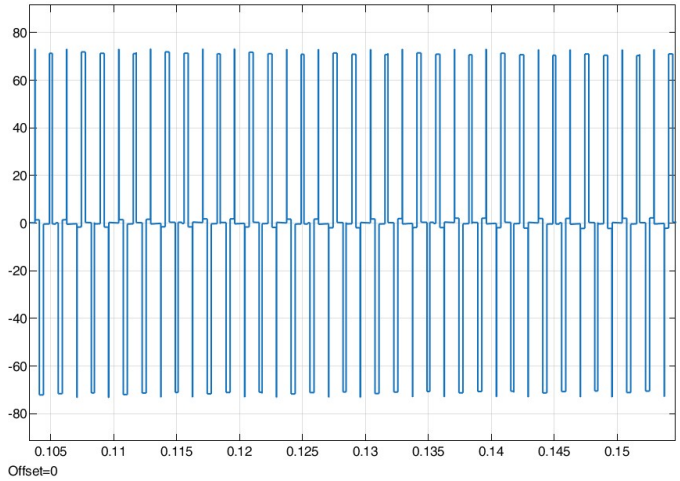


**Fig. 16.** CMV waveform for SHE. Periodic square pulses bounded at ±72 V demonstrate the lowest CMV of all three techniques, reducing insulation stress and leakage current risk.

TABLE IV

Common-Mode Voltage Stress Comparison

| Technique | Peak CMV (V) | Switching Freq. | EMI Risk |
|---|---|---|---|
| SHE | ±72 | 450 Hz | Minimal |
| PD-SPWM | ±225 | 5 kHz | High |
| SVPWM | >±300 | ~5 kHz | Critical |

### *D. Dynamic Performance Under Varying Irradiance*

Table V presents the THD under three irradiance conditions. Under a dynamic step from 1000 W/m² to 400 W/m², the P&O MPPT algorithm re-established the maximum power point within 0.05 s, maintaining DC-link voltage within 1.5% of the 800 V nominal. PD-SPWM maintained THD below 1.45% throughout, confirming robustness to DC-link ripple. SHE's THD remained below 3.12%, confirming that LUT angle interpolation provides sufficient transient stability. SVPWM's THD rose to 11.20% at 400 W/m² as lower modulation indices push V_ref into outer sub-hexagon regions where quantisation errors intensify. This dynamic degradation alone disqualifies SVPWM for grid-tied PV applications without a fundamentally different filter strategy.

TABLE V

Transient THD Under Varying Irradiance

| Irradiance | PD-SPWM THD (%) | SHE THD (%) | SVPWM THD (%) |
|---|---|---|---|
| 1000 W/m² (Steady) | 1.01 | 2.69 | 8.43 |
| 400 W/m² (Low Light) | 1.45 | 3.12 | 11.20 |
| Recovery (800 W/m²) | 1.08 | 2.75 | 9.15 |

### *E. Consolidated Performance Comparison*

Table VI consolidates all metrics. PD-SPWM is the superior choice where power quality is the primary constraint: lowest THD (1.01%), highest VUF (49.75%), and strong dynamic robustness. SHE is the thermally optimal choice for utility-scale deployment: lowest CMV (±72 V), lowest switching frequency (450 Hz), and a smaller required LCL filter. SVPWM fails both THD compliance and VUF targets and is unsuitable for grid-tied PV in the five-level NPC configuration with the LCL filter parameterised for carrier-based methods.

TABLE VI

Consolidated Performance Matrix

| Metric | PD-SPWM | SVPWM | SHE |
|---|---|---|---|
| Filtered THD (%) | 1.01 (Best) | 8.43 (Fail) | 2.69 |
| Dynamic THD at 400 W/m² (%) | 1.45 | 11.20 | 3.12 |
| Peak CMV (V) | ±225 | >±300 | ±72 (Best) |
| VUF (%) | 49.75 (Best) | 28.71 | 37.20 |
| Switching Frequency | 5 kHz | ~5 kHz | 450 Hz (Best) |
| IEEE 1547 Compliance | Pass | Fail | Pass |

  

unchanged from the 15 µF case, because the VUF shortfall is algorithmic. SVPWM therefore remains unsuitable for the present design, but a purpose-designed filter that accepts a lower resonant frequency can recover its THD compliance, a trade-off quantified here for the first time.

### *F. SVPWM Filter Sensitivity*

The 8.43% filtered-THD failure reported for SVPWM (Table II) was obtained with the LCL filter parameterised for the carrier-based methods ($C^f$ = 15 µF). To test whether this non-compliance is intrinsic to SVPWM or an artefact of filter tuning, the filter capacitance was increased tenfold to $C^f$ = 150 µF and the steady-state case re-simulated. The SVPWM filtered THD then falls to 1.68% (Fig. 17), within the IEEE 1547 5% limit, confirming that the failure is filter-bound rather than fundamental to the modulation strategy. The improvement carries two penalties. First, raising $C^f$ by an order of magnitude lowers the LCL resonant frequency to f_res ≈ 159 Hz, violating the stability criterion 10·f_grid < f_res (500 Hz < f_res) used to size the original filter, and a 150 µF capacitor draws substantially higher reactive current for a larger, costlier component. Second, the re-tuning leaves the DC-bus utilisation deficit untouched: the output fundamental remains near 235 V (VUF ≈ 28%),

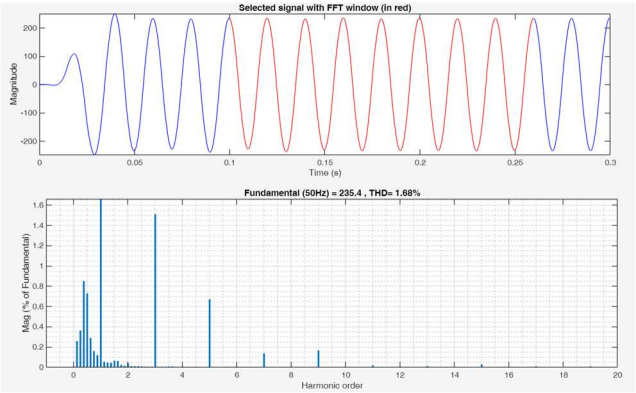


**Fig. 17.** SVPWM output with the re-tuned LCL filter ($C^f$ = 150 µF): output before (top) and after (bottom) filtering. Filtered THD falls to 1.68%, achieving IEEE 1547 compliance.

## V. Conclusion

This paper has presented the first simultaneous comparison of THD, CMV, and Voltage Utilisation Factor for PD-SPWM, SVPWM, and SHE applied to an identical three-phase five-level NPC grid-tied PV inverter. The principal findings are:

- PD-SPWM achieves 1.01% filtered THD and 49.75% VUF, providing the best power quality and DC-bus utilisation. Its high carrier frequency (5 kHz) increases thermal stress but makes it the preferred choice where stringent harmonic compliance is required.
- Under the LCL filter optimised for the carrier-based methods, five-level SVPWM is non-compliant with IEEE 1547 at 8.43% THD under steady state and 11.20% at low irradiance, with Section IV.F establishing that this is filter-bound: THD falls to 1.68% once the filter is sized for SVPWM. This cautions against extrapolating two-level SVPWM superiority predictions to five-level systems and motivates per-technique filter co-design rather than disqualification of SVPWM as a category.
- SHE achieves 2.69% filtered THD, the lowest peak CMV (±72 V), and operates at 450 Hz, reducing IGBT thermal cycling and PV panel insulation stress. It is the thermally optimal strategy for utility-scale PV deployment.
- N-R failure at extreme modulation indices (M < 0.4 and M > 0.95) reflects a known limitation of gradient-based solvers, which GA-based resolution overcomes across the full modulation range, supporting the use of global optimisation methods for LUT generation; benchmarking GA against other modern metaheuristics remains future work.

Future work should investigate: (a) active damping and LCL re-tuning for five-level SVPWM to achieve IEEE 1547 compliance without compromising resonant-frequency stability; (b) adaptive SHE using ANN interpolation to reduce harmonic transients at LUT boundary transitions; (c) fault ride-through performance under grid voltage sag; and (d) Model Predictive Control as a unified framework for five-level NPC inverter.

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