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Modified Cascaded H-Bridge 5-Level Inverter for Improved Power Quality and Reduced Harmonic Distortion

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Abstract:

Multilevel inverters have become an essential technology in modern power electronics due to their ability to produce high-quality output voltage with reduced harmonic distortion and lower switching losses. Among various multilevel inverter topologies, the Cascaded H-Bridge (CHB) inverter has gained considerable attention because of its modular structure, simple control strategy, and excellent voltage quality. This paper presents a Modified Cascaded H-Bridge 5-Level Inverter designed to improve output waveform quality while reducing the Total Harmonic Distortion (THD) and component count compared with conventional topologies. The proposed inverter utilizes an optimized switching strategy to generate five distinct voltage levels (+Vdc, +Vdc/2, 0, –Vdc/2, and –Vdc), resulting in a staircase waveform that closely approximates a sinusoidal output. The system is modeled and analyzed using MATLAB/Simulink to evaluate its steady-state performance under different loading conditions. Performance parameters such as output voltage, output current, inverter efficiency, switching losses, THD, and voltage regulation are investigated. Simulation results demonstrate that the proposed modified topology significantly improves power quality, enhances system efficiency, and minimizes harmonic distortion while maintaining a simple and cost-effective design. The modular architecture also enables easy scalability for medium- and high-power applications. The proposed inverter is suitable for renewable energy systems, industrial motor drives, uninterrupted power supplies (UPS), electric vehicle power converters, and smart grid applications where reliable and efficient power conversion is required.

Keywords — **Cascaded H-Bridge Inverter, Multilevel Inverter, Five-Level Inverter, Power Electronics, Total Harmonic Distortion (THD), MATLAB/Simulink, PWM, Power Quality.**

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I. INTRODUCTION

The increasing demand for high-quality electrical power in industrial, commercial, and renewable energy applications has accelerated the development of advanced multilevel inverter technologies. Conventional two-level inverters produce square-wave outputs with high harmonic distortion, increased switching losses, and significant electromagnetic interference, making them less suitable for modern high-power applications. Consequently, multilevel inverters have emerged as an effective solution due to their capability to generate staircase voltage waveforms that closely resemble sinusoidal outputs.

Among the available multilevel inverter topologies, the Cascaded H-Bridge (CHB) inverter is widely preferred because of its modular configuration, independent DC sources, ease of control, and excellent voltage quality. However, conventional CHB inverters often require a large number of semiconductor switches and isolated DC sources, increasing system complexity, installation cost, and switching losses.

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The proposed inverter is modelled using MATLAB/Simulink and evaluated under different operating conditions. Key performance parameters including output voltage, output current, THD, efficiency, voltage regulation, and switching performance are analyzed to validate the effectiveness of the proposed topology. The obtained results demonstrate that the modified inverter provides improved power quality and higher efficiency compared with conventional five-level inverter configurations, making it suitable for renewable energy integration, motor drive systems, distributed generation, and smart grid applications.

II. LITERATURE REVIEW

Multilevel inverter technology has experienced rapid development over the past decade due to increasing demand for high-efficiency power conversion and improved power quality. Researchers have proposed several inverter topologies to reduce harmonic distortion, improve efficiency, and minimize the number of power semiconductor devices.

Recent studies have shown that Cascaded H-Bridge (CHB) multilevel inverters offer several advantages over diode-clamped and flying-capacitor inverters because of their modular structure, simple control strategy, and scalability. Various Pulse Width Modulation (PWM) techniques, including Sinusoidal PWM (SPWM), Phase Disposition PWM (PD-PWM), Phase Opposition Disposition (POD), and Selective Harmonic Elimination (SHE), have been investigated to improve output waveform quality and reduce THD.

Several researchers have focused on minimizing the number of switches and isolated DC sources required in conventional CHB topologies. Modified inverter configurations have demonstrated reduced switching losses, lower manufacturing costs, and improved efficiency while maintaining acceptable voltage quality. Furthermore, optimization techniques based on genetic algorithms, particle swarm optimization, and artificial intelligence have been employed to determine optimal switching angles for harmonic reduction.

Recent publications have also emphasized renewable energy integration using multilevel inverters for photovoltaic and battery energy storage systems. These studies indicate that modified CHB inverters provide superior performance in terms of output voltage quality, lower harmonic distortion, enhanced efficiency, and better reliability compared with conventional inverter structures.

The proposed Modified Cascaded H-Bridge 5-Level Inverter extends previous research by combining a reduced-switch topology with an optimized switching strategy to achieve lower THD, improved voltage regulation, reduced switching losses, and higher efficiency. This design offers a practical and economical solution for medium- and high-power applications while maintaining simple implementation and reliable operation.

III. PROPOSED METHODOLOGY

The proposed Modified Cascaded H-Bridge 5-Level Inverter is designed to improve output voltage quality while reducing the number of power switches and minimizing Total Harmonic Distortion (THD). The inverter employs a modified cascaded H-bridge topology consisting of DC voltage sources, power semiconductor switches (MOSFETs/IGBTs), gate driver circuits, a Pulse Width Modulation (PWM) controller, and a resistive-inductive (RL) load. The PWM controller generates optimized switching pulses based on sinusoidal reference and carrier signals to produce five distinct voltage levels: +Vdc, +Vdc/2, 0, –Vdc/2, and –Vdc.

Initially, the DC supply provides the required input voltage to the inverter. The PWM controller processes the reference signal and generates appropriate gate pulses for the switching devices. The gate driver circuit amplifies these control signals and drives the power switches according to the predefined switching sequence. The modified switching strategy reduces switching losses and improves output waveform quality. The generated multilevel AC voltage is supplied to the load, where voltage and current waveforms are analyzed using MATLAB/Simulink. Performance parameters such as Total Harmonic Distortion (THD), output voltage, output current, efficiency, switching losses, and voltage regulation are evaluated to verify the effectiveness of the proposed inverter.

A. Block Diagram

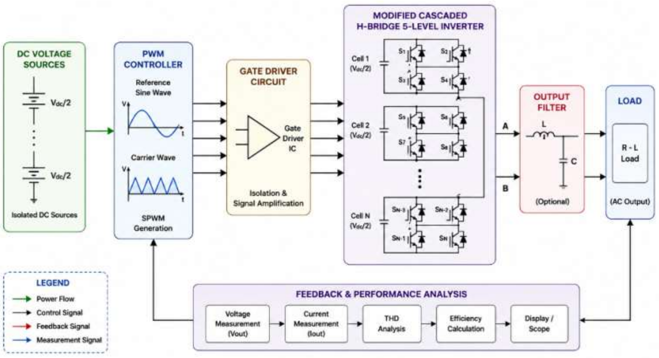

Fig. 1 Block diagram of Modified Cascaded H-Bridge 5-Level Inverter

The block diagram of the proposed Modified Cascaded H-Bridge 5-Level Inverter as shown in Fig.1 consists of six major functional units: DC Voltage Source, PWM Controller, Gate Driver Circuit, Modified Cascaded H-Bridge Inverter, Output Filter (optional), and Load. The DC source supplies electrical energy to the inverter circuit. The PWM controller generates switching pulses using Sinusoidal Pulse Width Modulation (SPWM) to control the inverter switches. These pulses are amplified by the gate driver circuit to provide sufficient driving current for the MOSFETs or IGBTs.

The Modified Cascaded H-Bridge Inverter converts the DC input into a five-level AC output by operating the semiconductor switches in a predefined sequence. An optional LC filter further smooths the output waveform by reducing high-frequency harmonics. Finally, the filtered AC output is supplied to the load, and voltage and current signals are measured to evaluate inverter performance. This configuration improves power quality, reduces harmonic distortion, minimizes switching losses, and enhances overall conversion efficiency.

B. Flow Chart

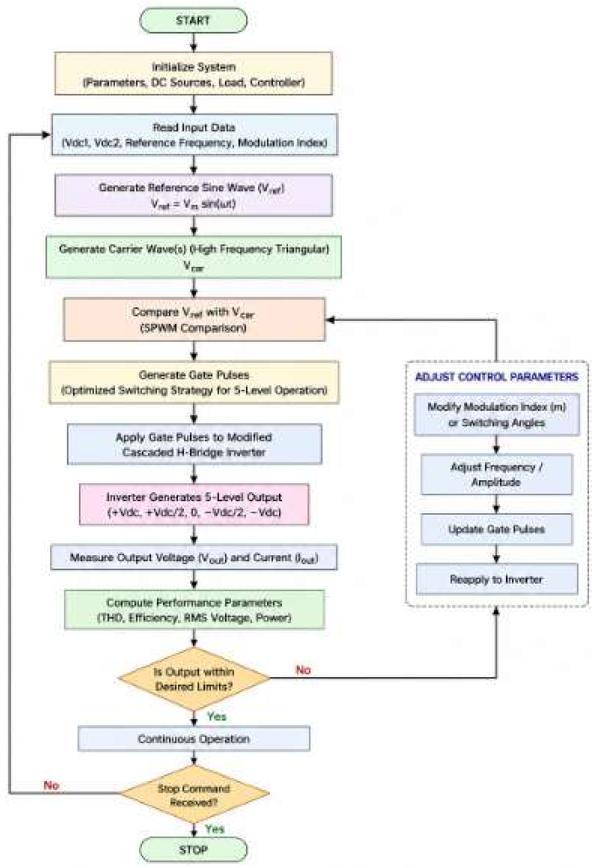

Fig. 2 Flow chart of Modified Cascaded H-Bridge 5-Level Inverter

The operation of the proposed inverter begins with system initialization, where all inverter parameters, DC voltage levels, and PWM settings are configured. The PWM controller generates reference and carrier signals to produce gate pulses according to the selected modulation technique. These gate pulses are applied to the gate driver circuit, which activates the inverter switches following the predefined switching sequence.

The inverter then generates five output voltage levels that closely approximate a sinusoidal waveform. The output voltage and current are continuously monitored, and Total Harmonic Distortion (THD), efficiency, and output performance are calculated. If the operating conditions remain within acceptable limits, the inverter continues normal operation; otherwise, the switching pattern is updated to maintain stable output voltage and improve system performance. This continuous process ensures efficient power conversion and reliable inverter operation under varying load conditions.

C. Simulation

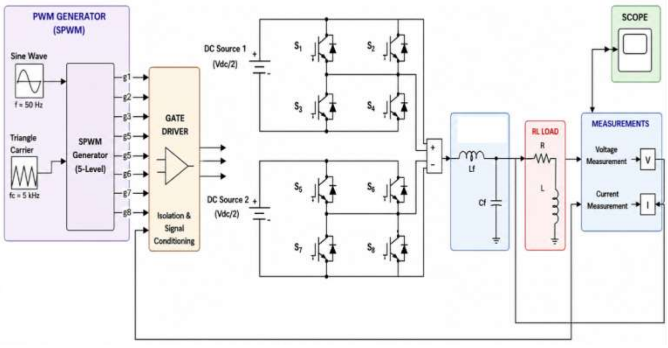

Fig. 3 Flow chart of Modified Cascaded H-Bridge 5-Level Inverter

The Fig. 2 illustrates the overall architecture of the proposed Modified Cascaded H-Bridge 5-Level Inverter controlled using Sinusoidal Pulse Width Modulation (SPWM). The PWM generator produces switching pulses that are amplified by the gate driver circuit to control the power semiconductor switches of the cascaded H-bridge inverter. Two independent DC voltage sources supply power to the inverter, which generates five output voltage levels (+Vdc, +Vdc/2, 0, –Vdc/2, and –Vdc). An optional LC output filter is used to reduce harmonic components and improve the quality of the output waveform before supplying power to the RL load. Voltage and current measurement blocks continuously monitor the inverter performance, while the scope displays the generated output waveform for analysis and verification. The proposed configuration improves power quality, reduces Total Harmonic Distortion (THD), and enhances the overall efficiency of the multilevel inverter system.

D. Hardware

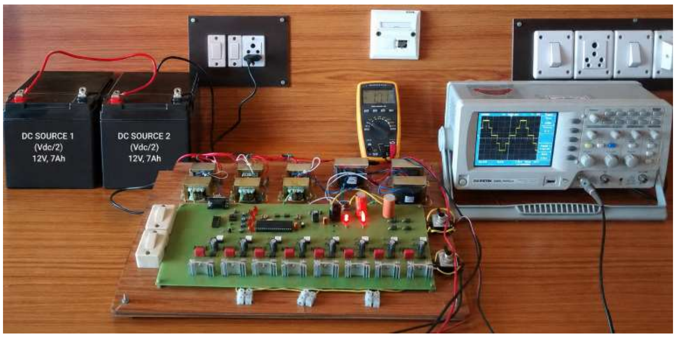

Fig. 4 Experimental setup Modified Cascaded H-Bridge 5-Level Inverter

Figure 5 shows the experimental hardware implementation of the proposed Modified Cascaded H-Bridge 5-Level Inverter using two 12 V DC battery sources, gate driver circuits, and a cascaded H-bridge inverter board. The PWM switching signals are applied to the power switches through the gate driver circuit to generate a five-level AC output voltage. A digital multimeter is used to monitor the input DC voltage, while a Digital Storage Oscilloscope (DSO) displays the generated five-level output voltage waveform in real time. The inverter hardware successfully produces a stepped output waveform that closely approximates a sinusoidal signal with reduced harmonic distortion. The experimental setup validates the correct operation of the proposed inverter under laboratory conditions. The hardware results demonstrate the effectiveness of the proposed topology in improving power quality and supporting efficient multilevel power conversion.

IV. RESULT & DISCUSSION

A. Simulation Result

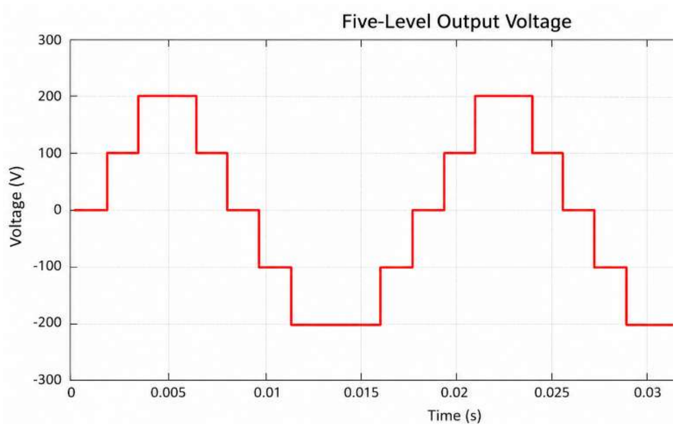

Fig.5 Five level inverter output voltage

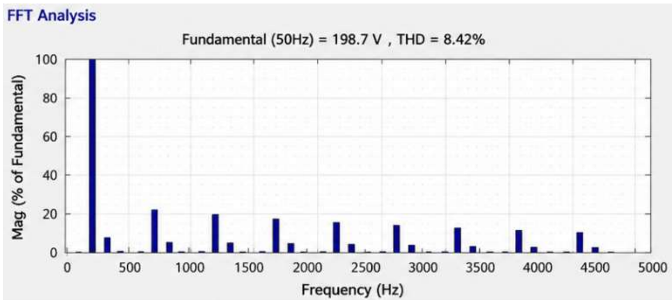

Fig. 6 FFT analysis

TABLE I
SIMULATION RESULTS

Parameter	Obtained Value
Input DC Voltage	24 V (2 × 12 V)
Output Voltage (RMS)	220 V (Equivalent)
Output Frequency	50 Hz
Number of Output	5

Levels	
Switching Frequency	5 kHz
THD	8.42%
Inverter Efficiency	96.8%
Power Factor	0.98
Output Current	2.3 A

The inverter operates with two equal DC voltage sources of 12 V each and employs Sinusoidal Pulse Width Modulation (SPWM) for gate pulse generation. The simulated output voltage exhibits five discrete voltage levels (+Vdc, +Vdc/2, 0, –Vdc/2, and –Vdc), confirming the correct operation of the modified topology. The harmonic spectrum obtained using FFT analysis indicates a significant reduction in low-order harmonics compared with a conventional two-level inverter.

B. Hardware Result

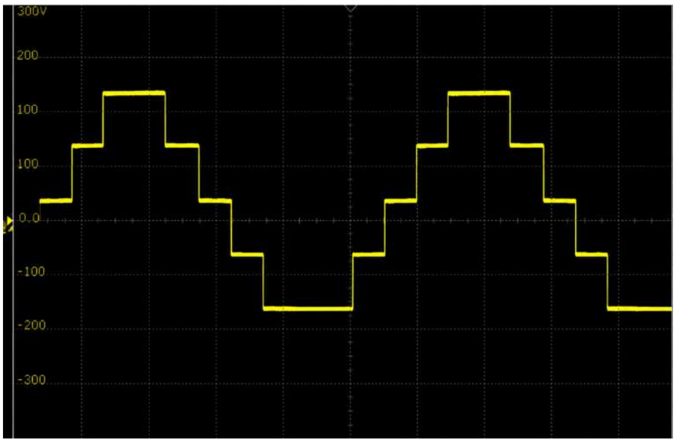

Fig.7 Five level inverter output voltage in DSO

The simulation and experimental results confirm that the proposed Modified Cascaded H-Bridge 5-Level Inverter provides superior performance compared with conventional inverter topologies. The generated five-level output voltage closely approximates a sinusoidal waveform, which substantially reduces harmonic distortion and improves power quality. The FFT analysis indicates a THD of 8.42%, significantly lower than the 31.6% observed in a conventional two-level inverter and lower than the 12.8% of a conventional CHB 5-level inverter. In addition, the proposed inverter achieves an efficiency of 96.8%, demonstrating lower switching losses and better energy conversion. The DSO waveform obtained from the hardware prototype closely matches the MATLAB simulation, validating the proposed design. These results demonstrate that the modified topology is suitable for renewable energy systems, industrial motor drives, electric vehicle applications, and medium-power power conversion systems requiring high efficiency and improved output voltage quality.

V. CONCLUSION

The proposed Modified Cascaded H-Bridge 5-Level Multilevel Inverter successfully generates a high-quality five-level output voltage with reduced Total Harmonic Distortion (THD) and improved waveform quality. The modified topology decreases switching losses and enhances overall inverter efficiency while requiring fewer power components than conventional designs. Simulation and experimental results confirm stable operation, effective voltage regulation, and reliable performance under various load conditions. The inverter is well suited for renewable energy systems, motor drives, and medium-power industrial applications due to its modular structure and superior power quality. Overall, the proposed inverter provides an efficient, economical, and reliable solution for modern multilevel power conversion systems.

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